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DISCLOSED TO:

TITLE:

COMPANY:

DATE:

DISCLOSED BY:

TITLE:

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MODIFICATION SHEET

Mods from 1.06 to 2.00

1) EBGA(Metal) Geode changed to TEBGA(Plastic) Geode
2) Renamed ON5V# to ON5V
3) Renamed ON-12V# to ON-12V
4) Made R94 a NL and R100 a 1K06SM
5) Remove Y10
6) Changed Tri-Media for BSP15
7) Changed DOC to G3 BGA type
8) Removed analog prep and Modulator.
9) Changed tuners to plug in headers
10) Changed the video buffers to more common type.
11) Changed the analog regs in accordance with new video buffers

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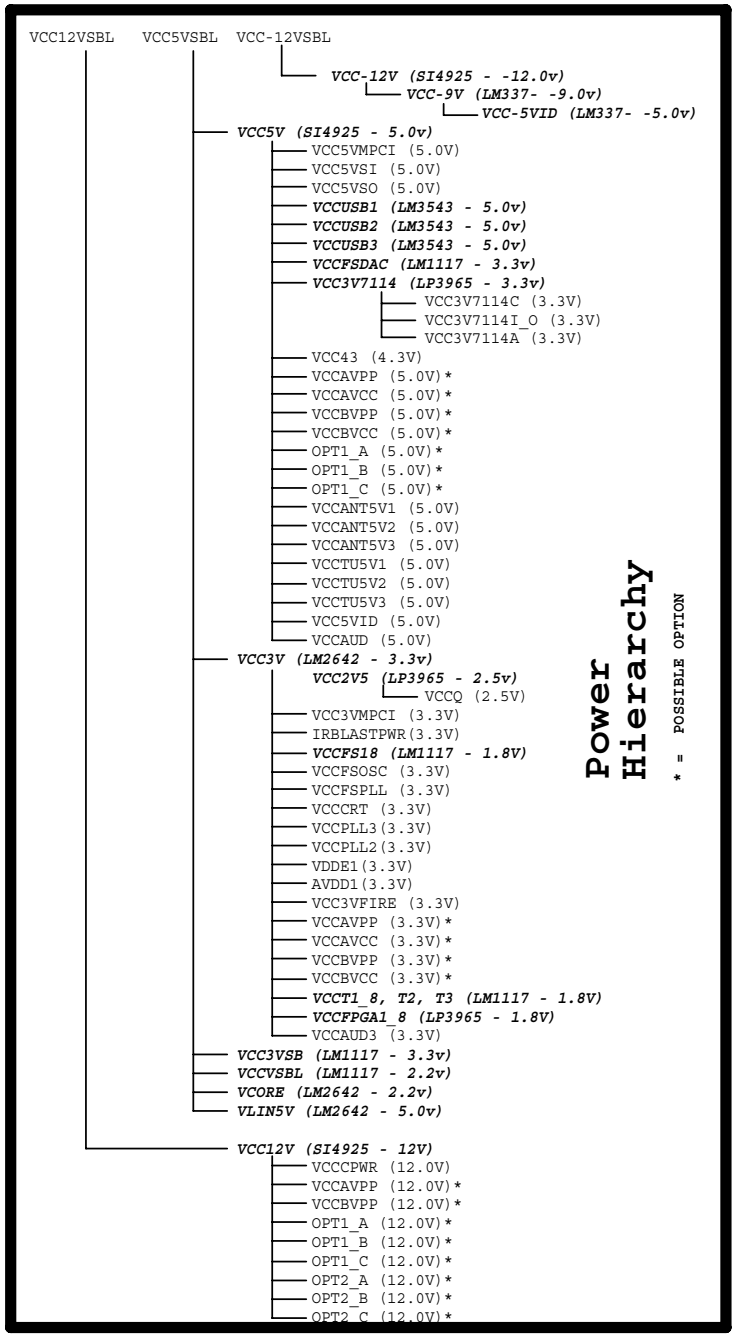

TEST	NET Name	DESCRIPTION	Volt	MAX I	Type
VTP1	VCC-12VSBL	Power In	-12.0v	300mA	R
VTP2	VCC5VSBL	Power In	5.0v	7.5A	R
VTP3	VCC12VSBL	Power In	12v	2.5A	R
VTP4	VCCVSBL	2.1v Standby	2.1V	68mA	R
VTP5	VCC3VSB	3.3v Standby	3.3v	80mA	R
VTP6	VLIN5V	LM2645 LDO	5.0v	100mA	R
VTP7	VCORE	2.1V Switched	2.1V	1.4A	R
VTP8	VCC3V	3.3V Switched	3.3v	5A	R
VTP9	VCC5V	Filtered Power In	5.0v	7.5A	R
VTP10	VCC-12V	Filtered Power In	-12.0v	300mA	R
VTP11	VCC-9V	VIDEO SUPPLY	-9.0v	330mA	R
VTP12	VCC-5VID	VIDEO SUPPLY	-5.0v	600mA	R
VTP13	VCCUSB1	USB SKT Supply	5.0v	500mA	S
VTP14	VCCUSB2	USB SKT Supply	5.0v	500mA	S
VTP15	VCCUSB3	USB SKT Supply	5.0v	500mA	S
VTP16	VCCFSDAC	VID DEC ANALOGUE	3.3v	200mA	R
VTP17	VCC3V7114	VID ENC ANALOGUE	3.3v	30mA	R
VTP18	VCC2V5	Trimedia 2.5v	2.5v	1.5A	R
VTP19	VCCFS18	VID DEC CORE	1.8v	75mA	R
VTP20	VCCT1_8	Tuner Supply	1.8v	260mA	R
VTP21	VCCFPGA1_8	FPGA CORE	1.8v	500mA	R
VTP22	VCC12V	Filtered Power In	12.0v	2.5A	R
VTP23	VCC5VMPCI	Mini PCI 5v	5.0v	200mA	F
VTP24	VCC5VSI	SPDIF 5v	5.0v	40mA	F
VTP25	VCC5VSO	SPDIF 5v	5.0v	40mA	F
VTP26	VCC3V7114C	VID ENC CORE	3.3v	30mA	F
VTP27	VCC3V7114I_O	VID ENC I/O	3.3v	30mA	F
VTP28	VCC3V7114A	VID ENC ANA	3.3v	70mA	F
VTP29	VCC43	IDE BUFFER	4.3v	5mA	F
VTP30	VCCAVPP	PCMCIA	12/5/3.3	XmA	S
VTP31	VCCAVCC	PCMCIA	12/5/3.3	XmA	S
VTP32	VCCBVPP	PCMCIA	12/5/3.3	XmA	S
VTP33	VCCBVCC	PCMCIA	12/5/3.3	XmA	S
VTP34	OPT1_A	TUNER OPTION	12/5	XmA	F
VTP35	OPT1_B	TUNER OPTION	12/5	XmA	F
VTP36	OPT1_C	TUNER OPTION	12/5	XmA	F
VTP37	VCCANT5V1	TUNER ANT	5.0v	110mA	F
VTP38	VCCANT5V2	TUNER ANT	5.0v	110mA	F
VTP39	VCCANT5V3	TUNER ANT	5.0v	110mA	F
VTP40	VCCTU5V1	TUNER 5V	5.0v	150mA	F
VTP41	VCCTU5V2	TUNER 5V	5.0v	150mA	F
VTP42	VCCTU5V3	TUNER 5V	5.0v	150mA	F
VTP43	VCC5VID	VIDEO ANA	5.0v	600mA	F
VTP44	VCCAUD	AUDIO ANA	5.0v	600mA	F
VTP45	VCCQ	TM quite supply	2.5v	200mA	F
VTP46	VCC3VMPCI	Mini PCI 3v	3.3v	454mA	F
VTP47	IRBLASTPWR	IRDA	3.3v	40mA	F
VTP48	VCCFSOSC	VID DEC OSC	3.3v	10mA	F
VTP49	VCCFSPLL	VID DEC PLL	3.3v	10mA	F
VTP50	VCCCRT	SOC Supply	3.3v	200mA	F
VTP51	VCCPLL3	SOC Supply	3.3v	200mA	F
VTP52	VCCPLL2	SOC Supply	3.3v	200mA	F
VTP53	VDDE1	Ethernet	3.3v	200mA	F
VTP54	AVDD1	Ethernet	3.3v	200mA	F
VTP55	VCC3VFIRE	FIREWIRE MAIN	3.3v	?	F
VTP56	VCCAUD3	AUDIO DIG	3.3v	200mA	F
VTP57	VCCCPWR	FIREWIRE PHY	12-40	?	F
VTP58	VCCP3VD	FIREWIRE DIG	3.3v	?	R
VTP59	VCCP3VA	FIREWIRE ANA	3.3v	?	F

TP		
TP1	CMOS & RTC Clock	32.768Khz
TP2	GEODE Crystal	27.000Mhz
TP3	Ethernet Crystal	25.000Mhz
TP4	Firewire Crystal	24.576Mhz
TP5	Trimedia Oscillator Clock	48.000Mhz
TP6	SAA7114 Crystal	24.576Mhz
TP7	FS454 Crystal	27.000Mhz
TP8	SDRAM LOOP IN	XXX Mhz
TP9	SO-DIMM Clock 0	XXX Mhz
TP10	SO-DIMM Clock 1	XXX Mhz
TP11	PCI clock In	33.333Mhz
TP12	LPC PCI Clock	33.333Mhz
TP13	Ethernet PCI Clock	33.333Mhz
TP14	FIREWIRE PCI Clock	33.333Mhz
TP15	FPGA PCI Clock	33.333Mhz
TP16	Trimedia PCI Clock	33.333Mhz
TP17	Mini PCI Clock	33.333Mhz
TP18	Arbitor PCI Clock	33.333Mhz
TP19	Trimedia Memory Clock 0	144.00Mhz
TP20	Trimedia Memory Clock 1	144.00Mhz
TP21	AC97 bit clock	12.288Mhz
TP22	AC97 clock	24.576Mhz
TP23	TUNER 1 Clock	XXX Mhz
TP24	TUNER 2 Clock	XXX Mhz
TP25	VID TRI TO GEODE	XXX Mhz
TP26	VID FPGA TO TM	XXX Mhz
TP27	VID TM TO FPGA	XXX Mhz
TP28	VID FPGA TO FS454 0	XXX Mhz
TP29	VID FPGA TO FS454 1	XXX Mhz
TP30	VID FS454 TO FPGA	XXX Mhz
TP31	VID SAA7114 TO FPGA	XXX Mhz
TP32	VID GEODE TFT TO FPGA	XXX Mhz

SYSTEM NOTES	
Silicon Revision	D2, D3
Maximum CPU Clock	300
Maximum Memory Speed	133
Maximum PCI Bus Speed	33 / 66
Low Power Susspend To RAM	NO
Single GND Plane	YES

TEST DATA

NL as suffix on part number means NO LOAD, don't fit part

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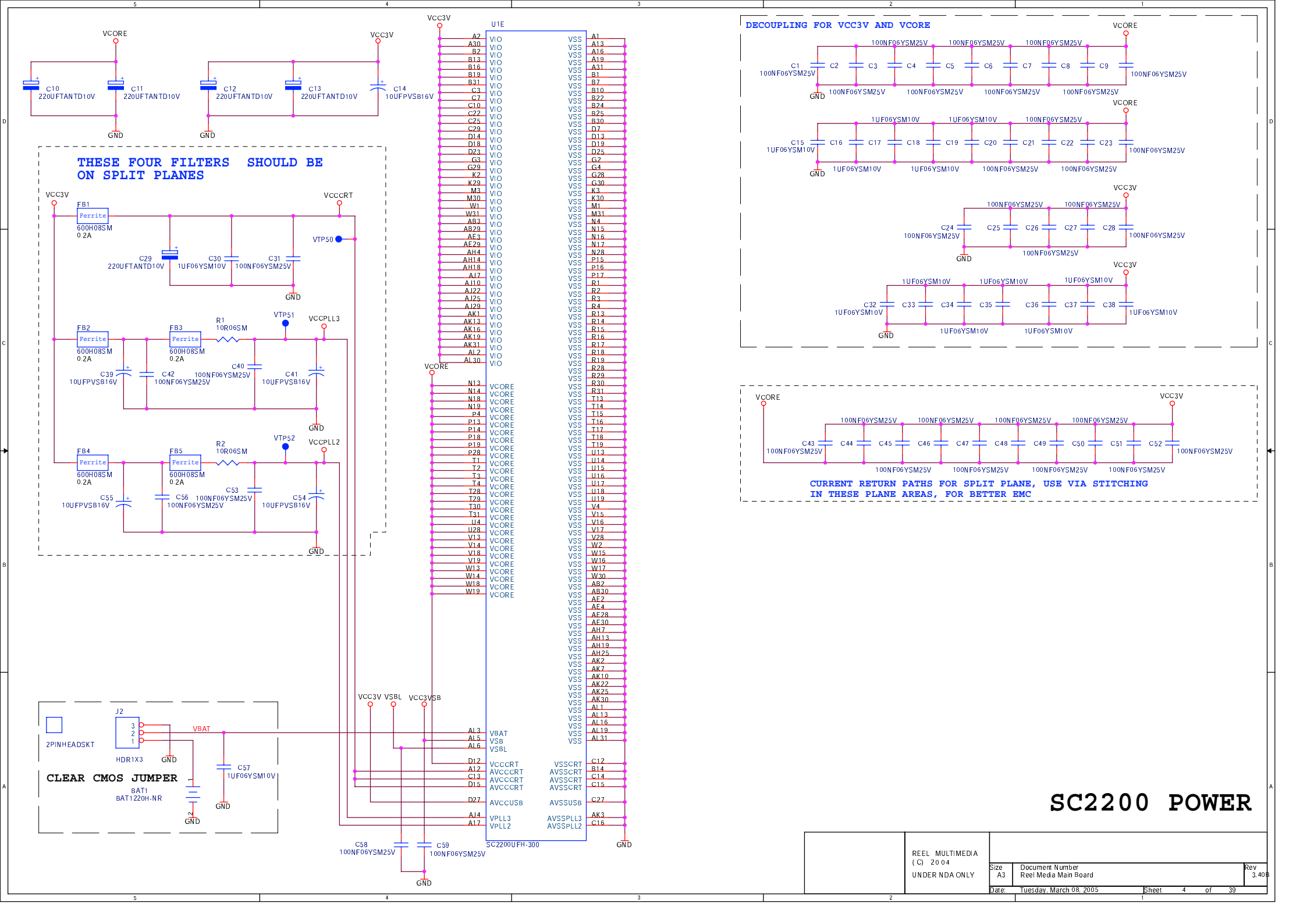
VCORE
VCC3V
U1E
C10 220UFTANTD10V
C11 220UFTANTD10V
C12 220UFTANTD10V
C13 220UFTANTD10V
C14 10UFPVSB16V
GND
THESE FOUR FILTERS SHOULD BE ON SPLIT PLANES
FB1 Ferrite 600H08SM 0.2A
FB2 Ferrite 600H08SM 0.2A
FB3 Ferrite 600H08SM 0.2A
FB4 Ferrite 600H08SM 0.2A
FB5 Ferrite 600H08SM 0.2A
VCCCRT
VTP50
VTP51
VTP52
VCCPLL3
VCCPLL2
R1 10R06SM
R2 10R06SM
C29 220UFTANTD10V
C30 1UF06YSM10V
C31 100NF06YSM25V
C39 10UFPVSB16V
C40 100NF06YSM25V
C41 10UFPVSB16V
C42 100NF06YSM25V
C53 100NF06YSM25V
C54 10UFPVSB16V
C55 10UFPVSB16V
C56 100NF06YSM25V
J2
2PINHEADSKT
HDR1X3
VBAT
CLEAR CMOS JUMPER
BAT1
BAT1220H-NR
C57 1UF06YSM10V
VSBL
VCC3VSB
C58 100NF06YSM25V
C59 100NF06YSM25V
SC2200UFH-300
DECOUPLING FOR VCC3V AND VCORE
C1 100NF06YSM25V
C2 C3 C4 C5 C6 C7 C8 C9 100NF06YSM25V
C15 1UF06YSM10V
C16 C17 C18 C19 C20 C21 C22 C23 100NF06YSM25V
C24 100NF06YSM25V
C25 C26 C27 C28 100NF06YSM25V
C32 1UF06YSM10V
C33 C34 C35 C36 C37 C38 1UF06YSM10V
C43 100NF06YSM25V
C44 C45 C46 C47 C48 C49 C50 C51 C52 100NF06YSM25V
CURRENT RETURN PATHS FOR SPLIT PLANE, USE VIA STITCHING IN THESE PLANE AREAS, FOR BETTER EMC
SC2200 POWER
REEL MULTIMEDIA
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Size A3
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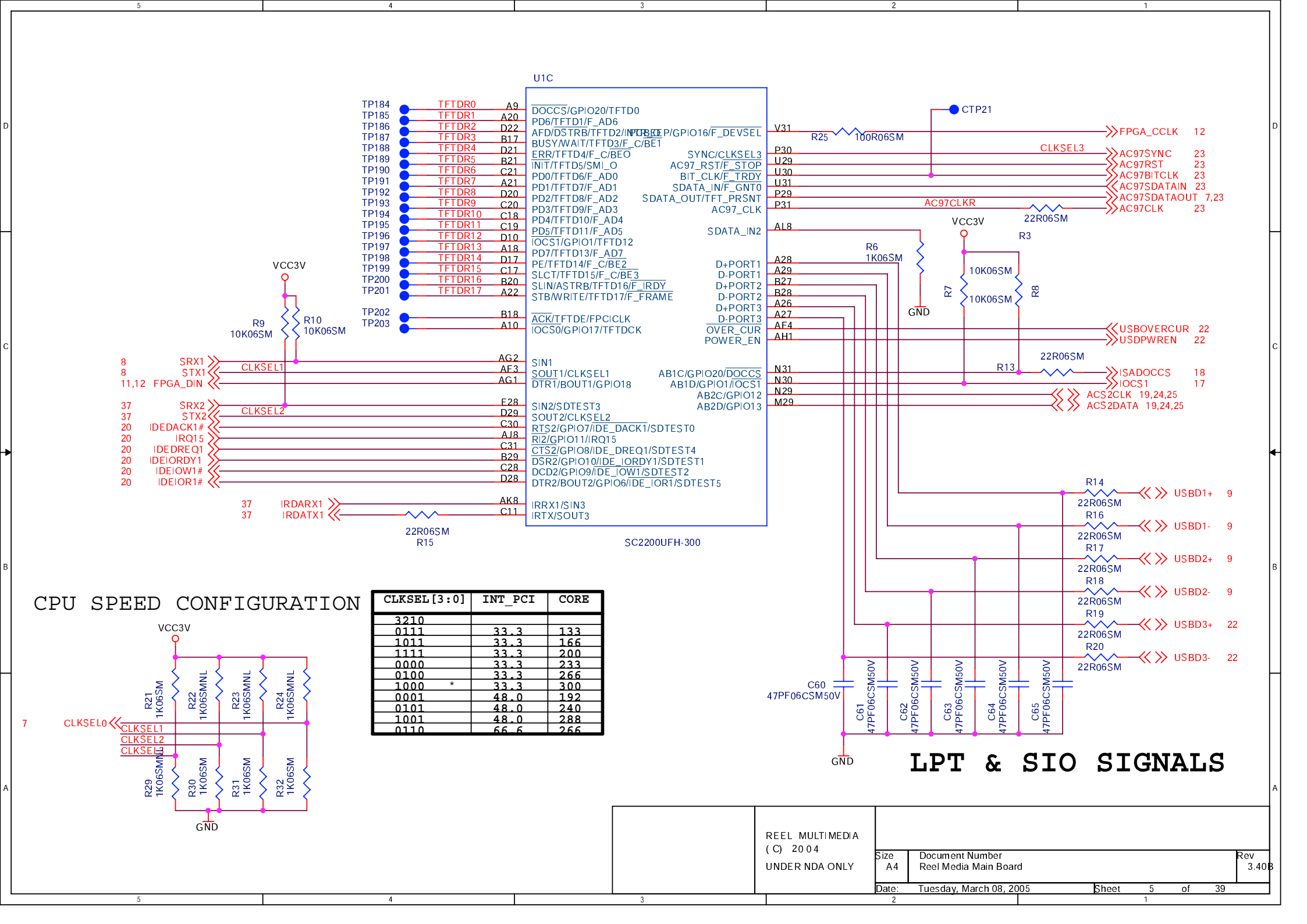

CLKSEL[3:0]		INT_PCI	CORE
3210			
0111		33.3	133
1011		33.3	166
1111		33.3	200
0000		33.3	233
0100		33.3	266
1000	*	33.3	300
0001		48.0	192
0101		48.0	240
1001		48.0	288
0110		66.6	266

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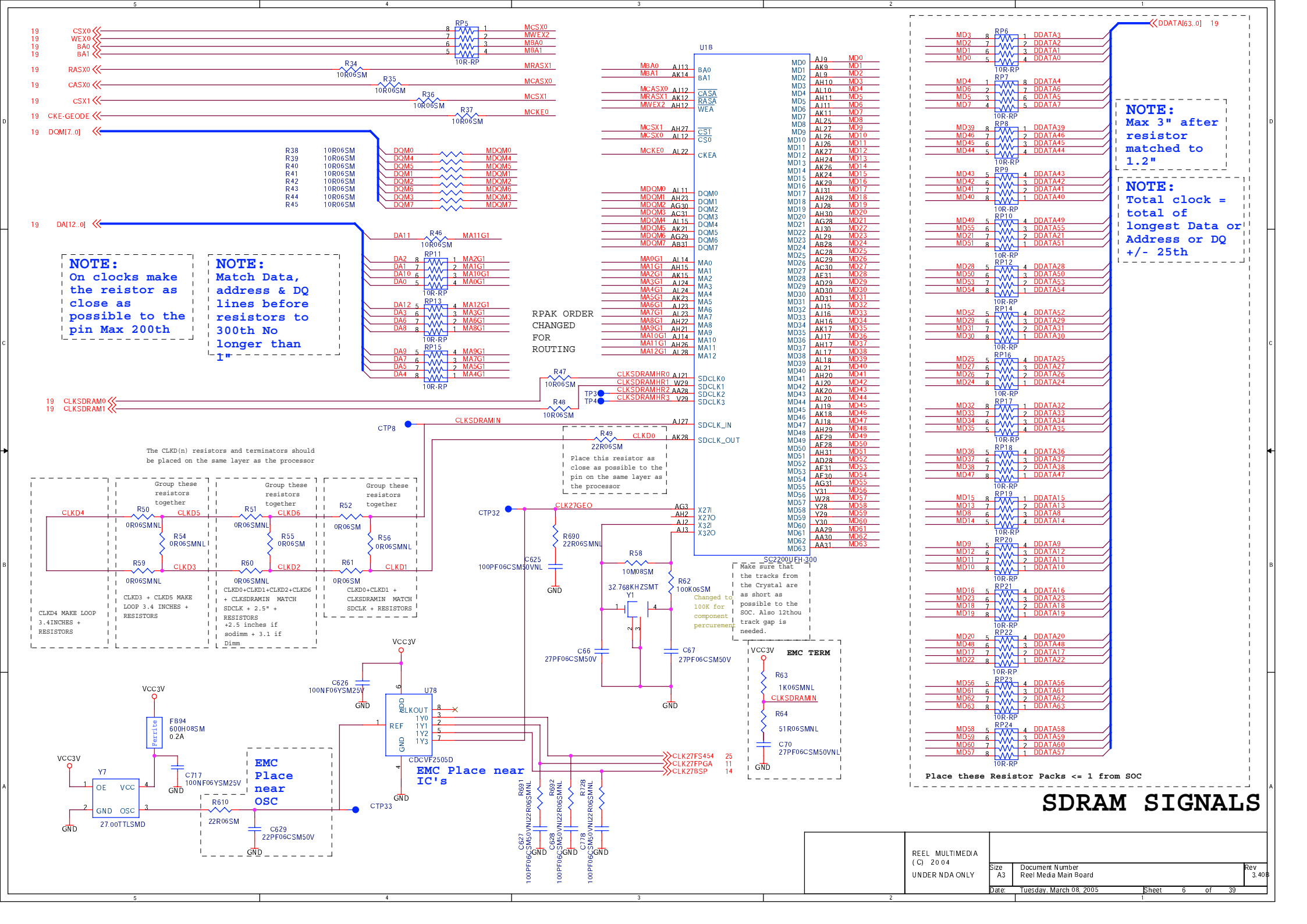
CSX0
WEX0
BA0
BA1
RASX0
CASX0
CSX1
CKE-GEODE
DQM[7..0]
DA[12..0]
CLKSDRAM0
CLKSDRAM1
RP5
10R-RP
MCSX0
MWEX2
MBA0
MBA1
MRASX1
MCASX0
MCSX1
MCKE0
R34 10R06SM
R35 10R06SM
R36 10R06SM
R37 10R06SM
R38 10R06SM
R39 10R06SM
R40 10R06SM
R41 10R06SM
R42 10R06SM
R43 10R06SM
R44 10R06SM
R45 10R06SM
DQM0
DQM4
DQM5
DQM1
DQM2
DQM6
DQM3
DQM7
MDQM0
MDQM4
MDQM5
MDQM1
MDQM2
MDQM6
MDQM3
MDQM7
DA11
R46 10R06SM
MA11G1
RP11
DA2
DA1
DA10
DA0
MA2G1
MA1G1
MA10G1
MA0G1
RP13
DA12
DA3
DA6
DA8
MA12G1
MA3G1
MA6G1
MA8G1
RP15
DA9
DA7
DA5
DA4
MA9G1
MA7G1
MA5G1
MA4G1
NOTE:
On clocks make the reistor as close as possible to the pin Max 200th
NOTE:
Match Data, address & DQ lines before resistors to 300th No longer than 1"
RPAK ORDER CHANGED FOR ROUTING
U1B
MBA0 AJ13
MBA1 AK14
MCASX0 AJ12
MRASX1 AK12
MWEX2 AH12
MCSX1 AH27
MCSX0 AL12
MCKE0 AL22
MDQM0 AL11
MDQM1 AH23
MDQM2 AG30
MDQM3 AC31
MDQM4 AL15
MDQM5 AK21
MDQM6 AG29
MDQM7 AB31
MA0G1 AL14
MA1G1 AH15
MA2G1 AK15
MA3G1 AJ24
MA4G1 AL24
MA5G1 AK23
MA6G1 AJ23
MA7G1 AL23
MA8G1 AH22
MA9G1 AH21
MA10G1 AJ14
MA11G1 AH26
MA12G1 AL28
BA0
BA1
CASA
RASA
WEA
CS0
CKEA
DQM0
DQM1
DQM2
DQM3
DQM4
DQM5
DQM6
DQM7
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
SDCLK0
SDCLK1
SDCLK2
SDCLK3
SDCLK_IN
SDCLK_OUT
MD0 AJ9
MD1 AK9
MD2 AL9
MD3 AH10
MD4 AL10
MD5 AH11
MD6 AJ11
MD7 AK11
MD8 AL25
MD9 AL27
MD10 AL26
MD11 AJ26
MD12 AK27
MD13 AH24
MD14 AK26
MD15 AK24
MD16 AK29
MD17 AJ31
MD18 AH28
MD19 AJ28
MD20 AH30
MD21 AG28
MD22 AJ30
MD23 AL29
MD24 AB28
MD25 AC28
MD26 AC29
MD27 AC30
MD28 AE31
MD29 AD29
MD30 AD30
MD31 AD31
MD32 AJ15
MD33 AJ16
MD34 AH16
MD35 AK17
MD36 AJ17
MD37 AH17
MD38 AL17
MD39 AL18
MD40 AL21
MD41 AH20
MD42 AJ20
MD43 AK20
MD44 AL20
MD45 AJ19
MD46 AK18
MD47 AJ18
MD48 AH29
MD49 AE29
MD50 AE28
MD51 AH31
MD52 AD28
MD53 AE31
MD54 AE30
MD55 AG31
MD56 Y31
MD57 W28
MD58 Y28
MD59 Y29
MD60 Y30
MD61 AA29
MD62 AA30
MD63 AA31
SC2200UFH-300
CLKSDRAMHR0 AJ21
CLKSDRAMHR1 W29
CLKSDRAMHR2 AA28
CLKSDRAMHR3 V29
R47 10R06SM
R48 10R06SM
TP3
TP4
CTP8
CLKSDRAMIN
AJ27
R49 22R06SM
CLKD0 AK28
Place this resistor as close as possible to the pin on the same layer as the processor
The CLKD(n) resistors and terminators should be placed on the same layer as the processor
CLKD4
CLKD5
CLKD6
CLKD3
CLKD2
CLKD1
R50 0R06SMNL
R51 0R06SMNL
R52 0R06SM
R54 0R06SMNL
R55 0R06SM
R56 0R06SMNL
R59 0R06SMNL
R60 0R06SMNL
R61 0R06SM
Group these resistors together
CLKD4 MAKE LOOP 3.4INCHES + RESISTORS
CLKD3 + CLKD5 MAKE LOOP 3.4 INCHES + RESISTORS
CLKD0+CLKD1+CLKD2+CLKD6 + CLKSDRAMIN MATCH SDCLK + 2.5" + RESISTORS +2.5 inches if sodimm + 3.1 if Dimm
CLKD0+CLKD1 + CLKSDRAMIN MATCH SDCLK + RESISTORS
CTP32
CLK27GEO
AG3
AH2
AJ2
AJ3
X27I
X27O
X32I
X32O
R690 22R06SMNL
C625 100PF06CSM50VNL
R58 10M08SM
32.768KHZSMT
Y1
R62 100K06SM
Changed to 100K for component percurement
Make sure that the tracks from the Crystal are as short as possible to the SOC. Also 12thou track gap is needed.
C66 27PF06CSM50V
C67 27PF06CSM50V
GND
VCC3V
EMC TERM
R63 1K06SMNL
CLKSDRAMIN
R64 51R06SMNL
C70 27PF06CSM50VNL
C626 100NF06YSM25V
U78
CDCVF2505D
VDD
CLKOUT
REF
1Y0
1Y1
1Y2
1Y3
GND
FB94 600H08SM 0.2A
Ferrite
C717 100NF06YSM25V
Y7
OE
VCC
GND
OSC
27.00TTLSMD
R610 22R06SM
C629 22PF06CSM50V
EMC Place near OSC
EMC Place near IC's
CTP33
CLK27FS454 25
CLK27FPGA 11
CLK27BSP 14
R691 R692 R728
C627 C628 C778
100PF06CSM50VNL22R06SMNL
DDATA[63..0] 19
RP6 RP7 RP8 RP9 RP10 RP12 RP14 RP16 RP17 RP18 RP19 RP20 RP21 RP22 RP23 RP24
MD3 MD2 MD1 MD0 DDATA3 DDATA2 DDATA1 DDATA0
MD4 MD6 MD5 MD7 DDATA4 DDATA6 DDATA5 DDATA7
MD39 MD46 MD45 MD44 DDATA39 DDATA46 DDATA45 DDATA44
MD43 MD42 MD41 MD40 DDATA43 DDATA42 DDATA41 DDATA40
MD49 MD55 MD21 MD51 DDATA49 DDATA55 DDATA21 DDATA51
MD28 MD50 MD53 MD54 DDATA28 DDATA50 DDATA53 DDATA54
MD52 MD29 MD31 MD30 DDATA52 DDATA29 DDATA31 DDATA30
MD25 MD27 MD26 MD24 DDATA25 DDATA27 DDATA26 DDATA24
MD32 MD33 MD34 MD35 DDATA32 DDATA33 DDATA34 DDATA35
MD36 MD37 MD38 MD47 DDATA36 DDATA37 DDATA38 DDATA47
MD15 MD13 MD8 MD14 DDATA15 DDATA13 DDATA8 DDATA14
MD9 MD12 MD11 MD10 DDATA9 DDATA12 DDATA11 DDATA10
MD16 MD23 MD18 MD19 DDATA16 DDATA23 DDATA18 DDATA19
MD20 MD48 MD17 MD22 DDATA20 DDATA48 DDATA17 DDATA22
MD56 MD61 MD62 MD63 DDATA56 DDATA61 DDATA62 DDATA63
MD58 MD59 MD60 MD57 DDATA58 DDATA59 DDATA60 DDATA57
NOTE:
Max 3" after resistor matched to 1.2"
NOTE:
Total clock = total of longest Data or Address or DQ +/- 25th
Place these Resistor Packs <= 1 from SOC
SDRAM SIGNALS
REEL MULTIMEDIA
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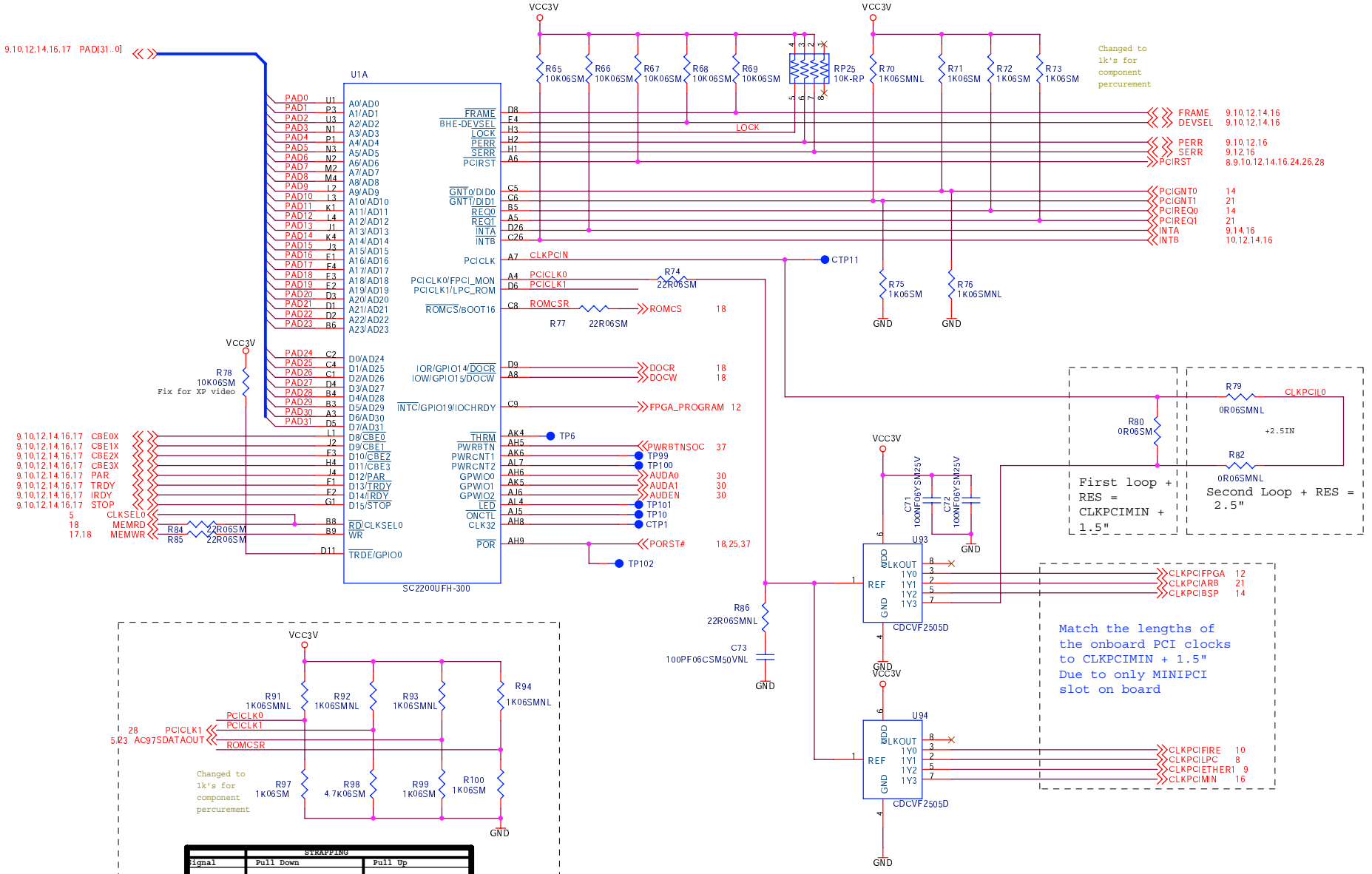

PCI SIGNALS

REEL MULTIMEDIA
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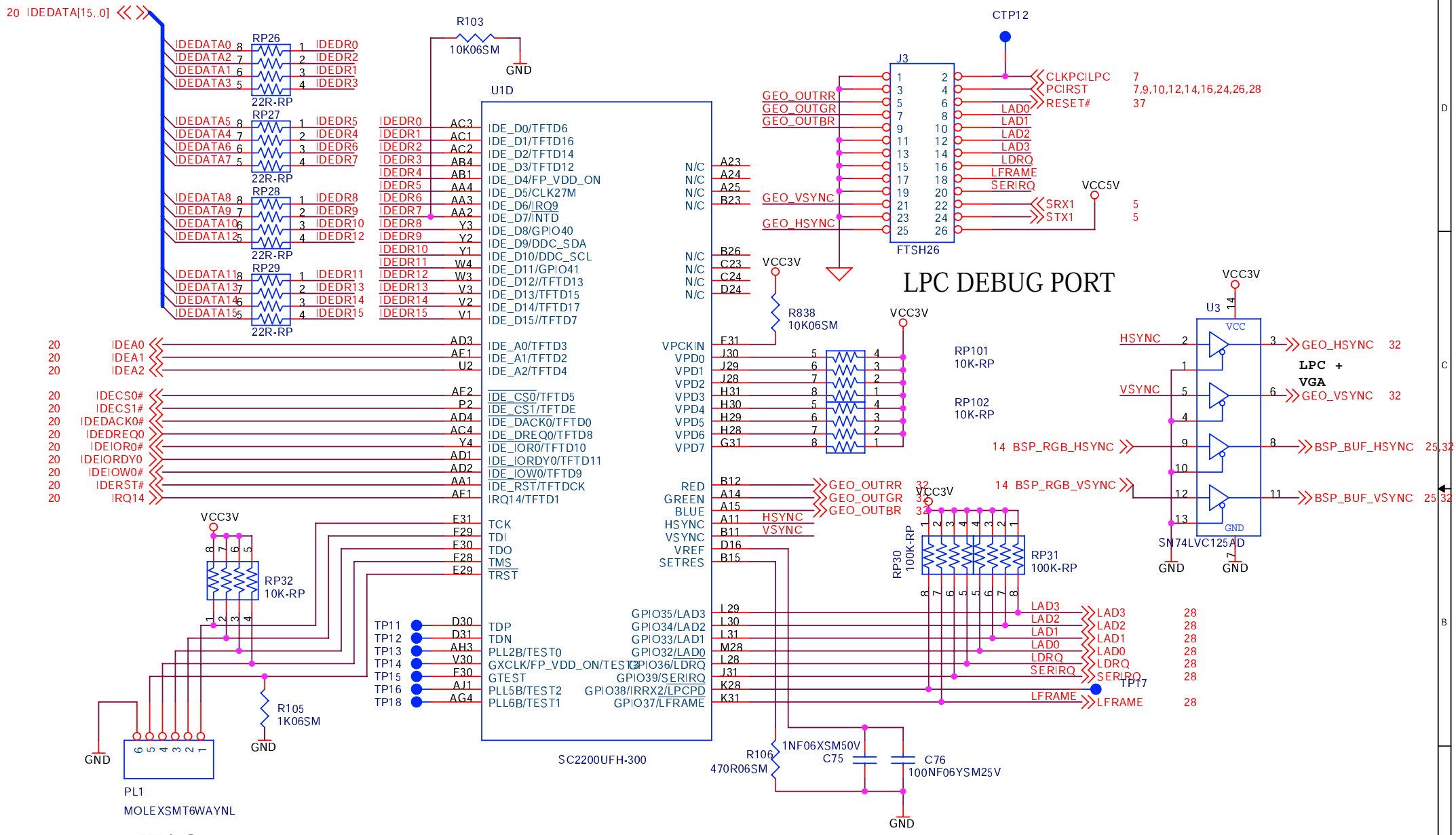

REEL MULTIMEDIA (C) 2004 UNDER NDA ONLY	Size A4	Document Number Reel Media Main Board	Rev 3.40B
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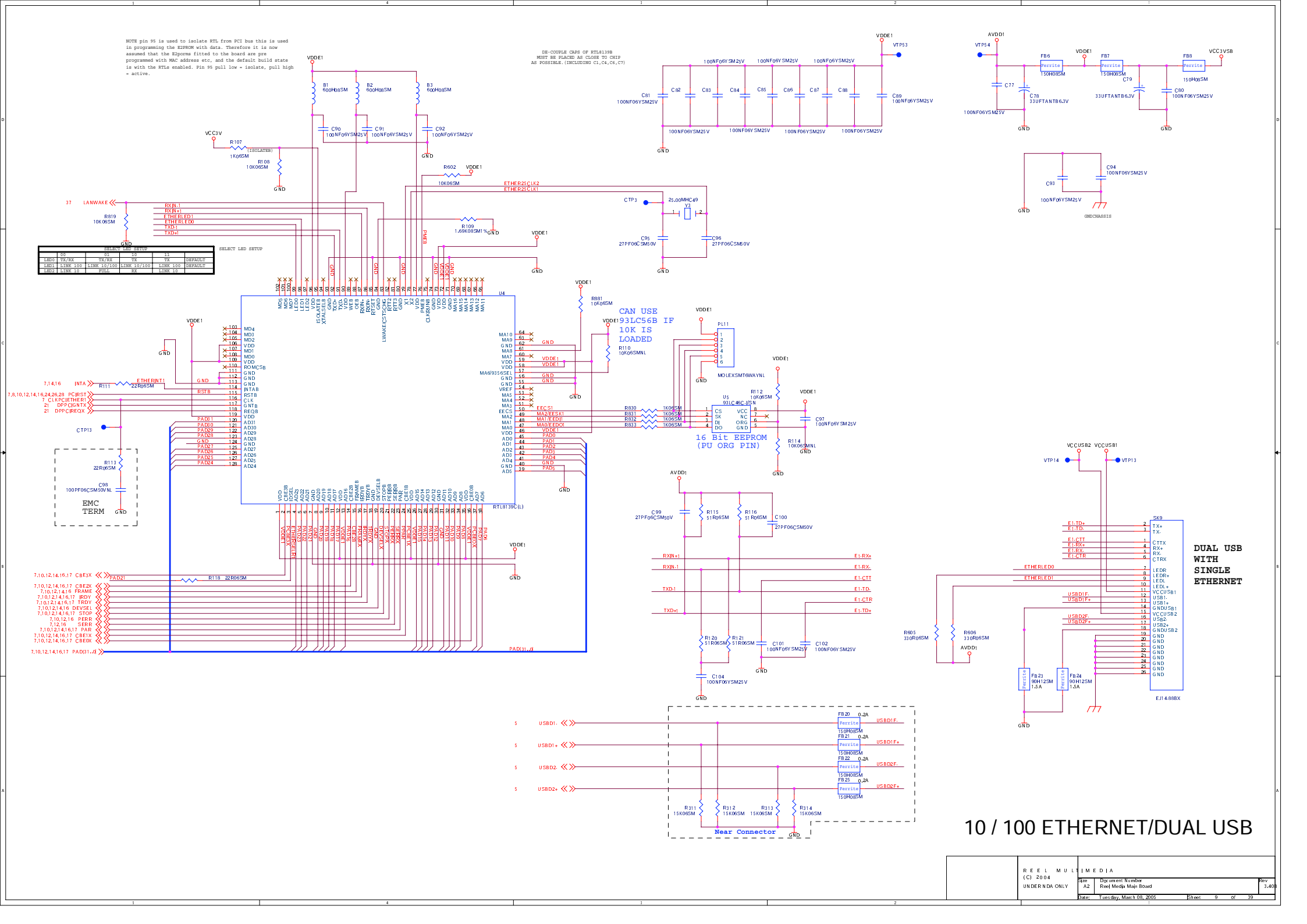
NOTE pin 95 is used to isolate RTL from PCI bus this is used in programming the EEPROM with data. Therefore it is now assumed that the EZporms fitted to the board are pre programmed with MAC address etc, and the default build state is with the RTLs enabled. Pin 95 pull low = isolate, pull high = active.
DE-COUPLE CAPS OF RTL8139B MUST BE PLACED AS CLOSE TO CHIP AS POSSIBLE.(INCLUDING C1,C4,C6,C7)
SELECT LED SETUP
CAN USE 93LC56B IF 10K IS LOADED
16 Bit EEPROM (PU ORG PIN)
EMC TERM
DUAL USB WITH SINGLE ETHERNET
Near Connector
10 / 100 ETHERNET/DUAL USB
REEL MULTIMEDIA
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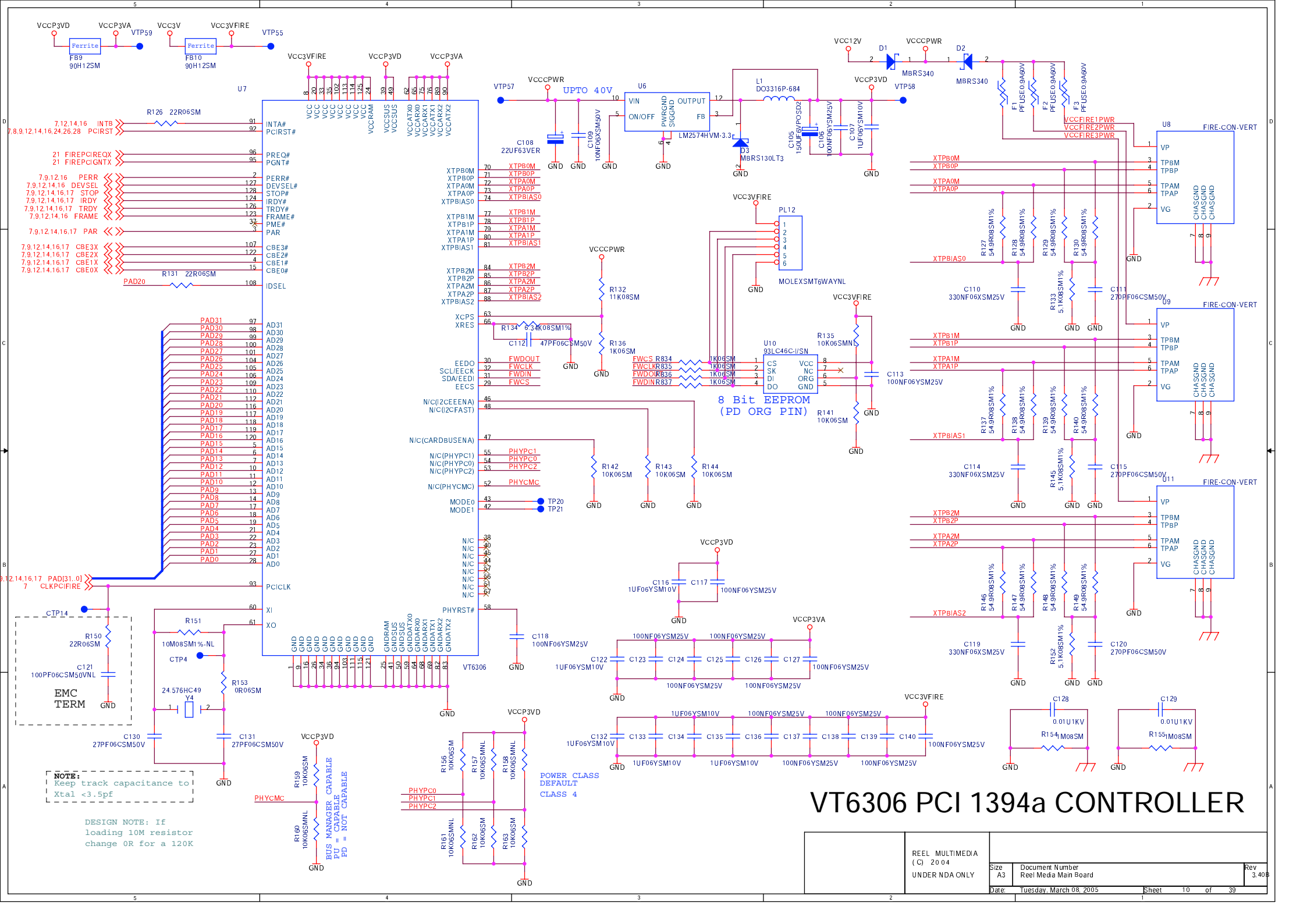
VT6306 PCI 1394a CONTROLLER
8 Bit EEPROM
(PD ORG PIN)
UPTO 40V
LM2574HVM-3.3
MOLEXSMT6WAYNL
FIRE-CON-VERT
EMC
TERM
NOTE:
Keep track capacitance to
Xtal <3.5pf
DESIGN NOTE: If
loading 10M resistor
change 0R for a 120K
POWER CLASS
DEFAULT
CLASS 4
BUS MANAGER CAPABLE
PU = CAPABLE
PD = NOT CAPABLE
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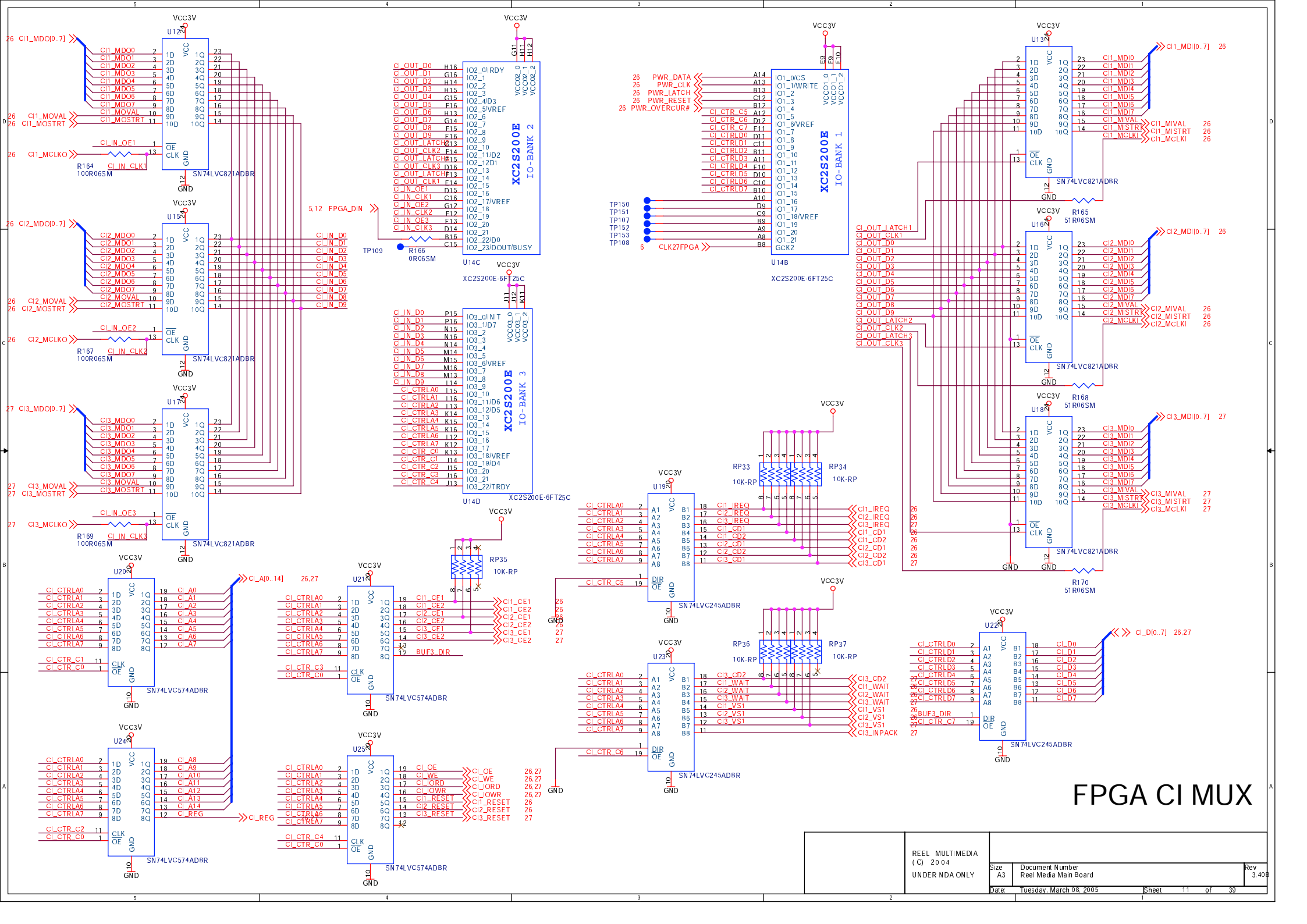
FPGA CI MUX
XC2S200E IO-BANK 2
XC2S200E IO-BANK 1
XC2S200E IO-BANK 3
XC2S200E-6FT25C
SN74LVC821ADBR
SN74LVC574ADBR
SN74LVC245ADBR
10K-RP
51R06SM
100R06SM
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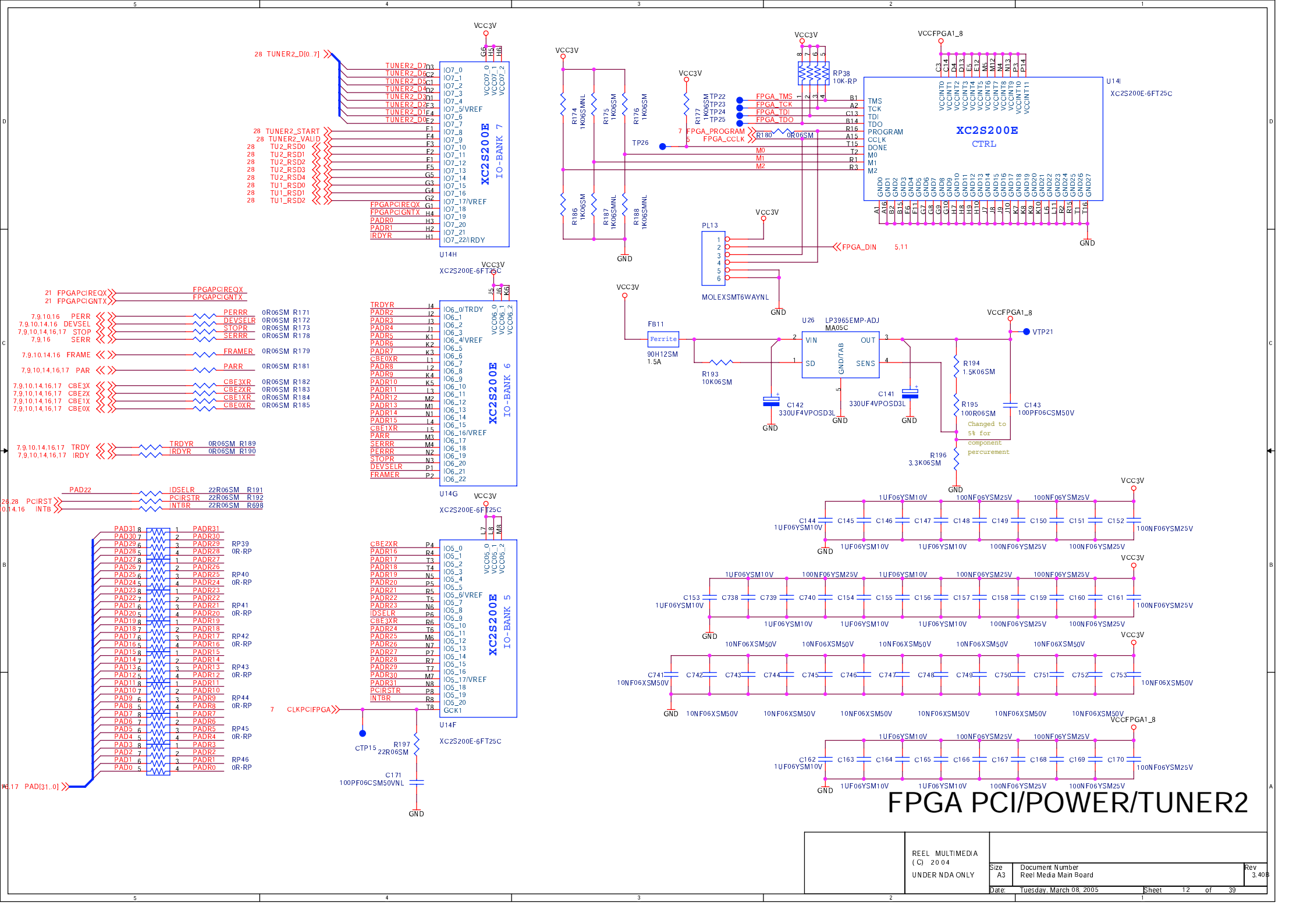
FPGA PCI/POWER/TUNER2
REEL MULTIMEDIA
(C) 2004
UNDER NDA ONLY
Size A3
Document Number
Reel Media Main Board
Rev 3.40B
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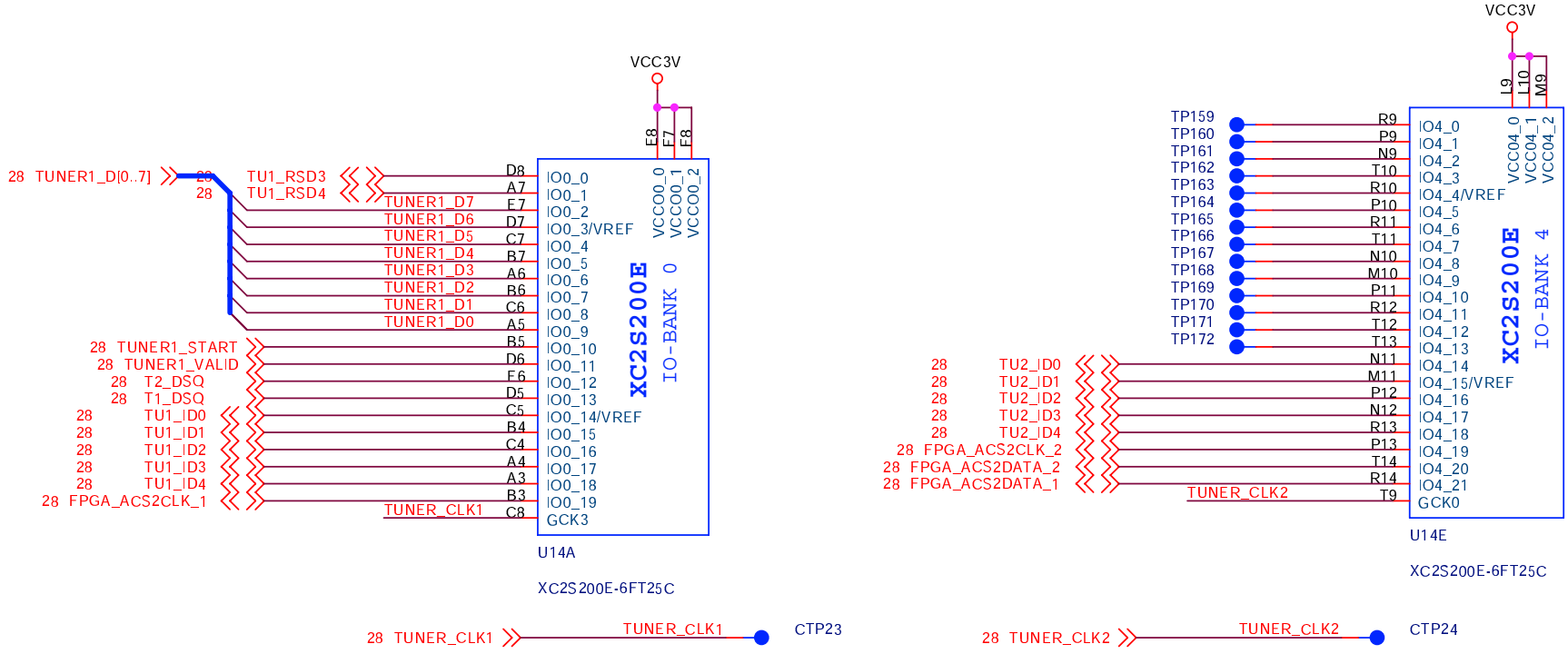
XC2S200E-6FT25C
XC2S200E
IO-BANK 7
IO-BANK 6
IO-BANK 5
CTRL
U14H
U14G
U14F
U14I
U26 LP3965EMP-ADJ
MA05C
MOLEXSMT6WAYNL
90H12SM
1.5A
Changed to 5% for component percurement



FPGA BSP/TUNER

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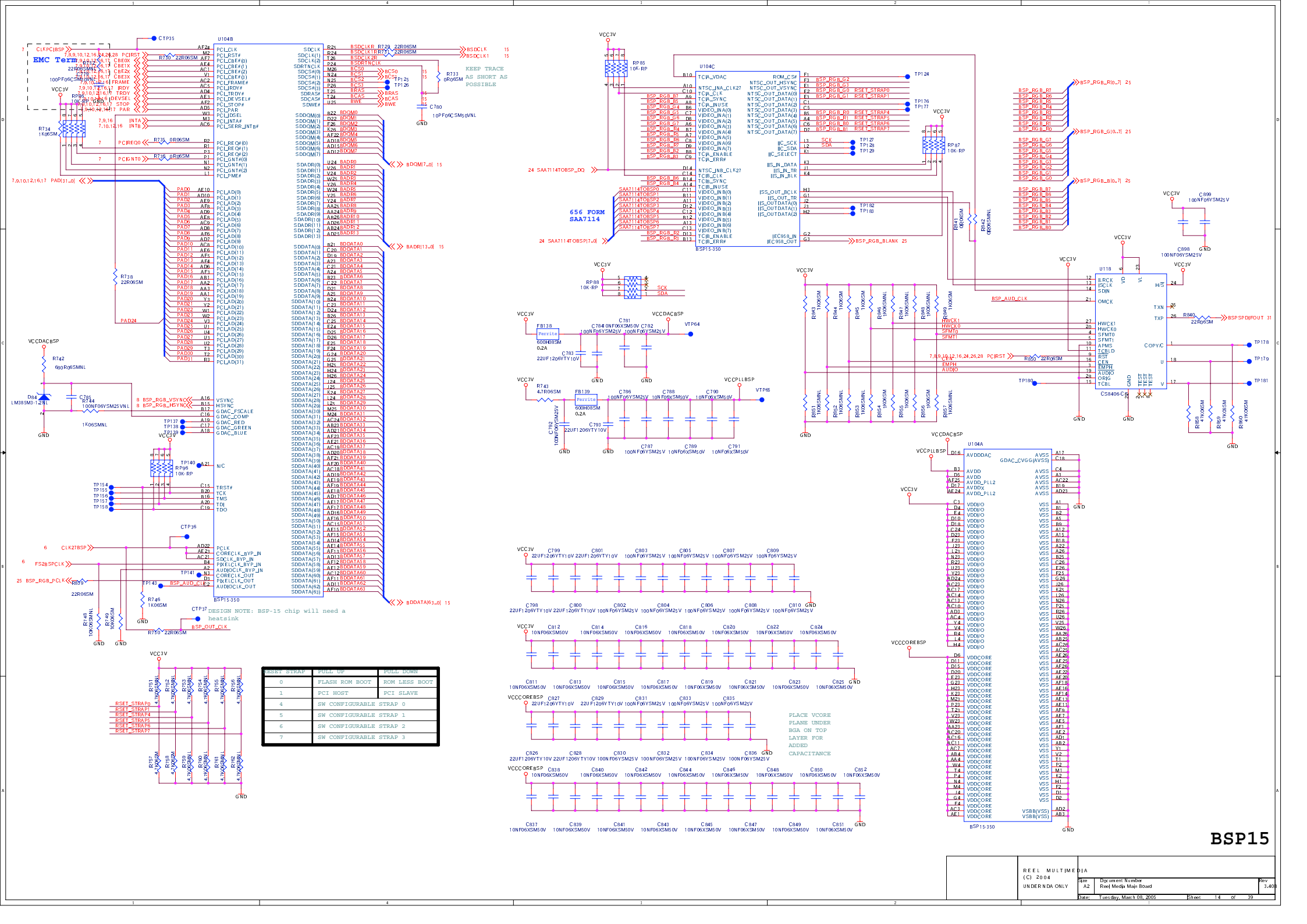
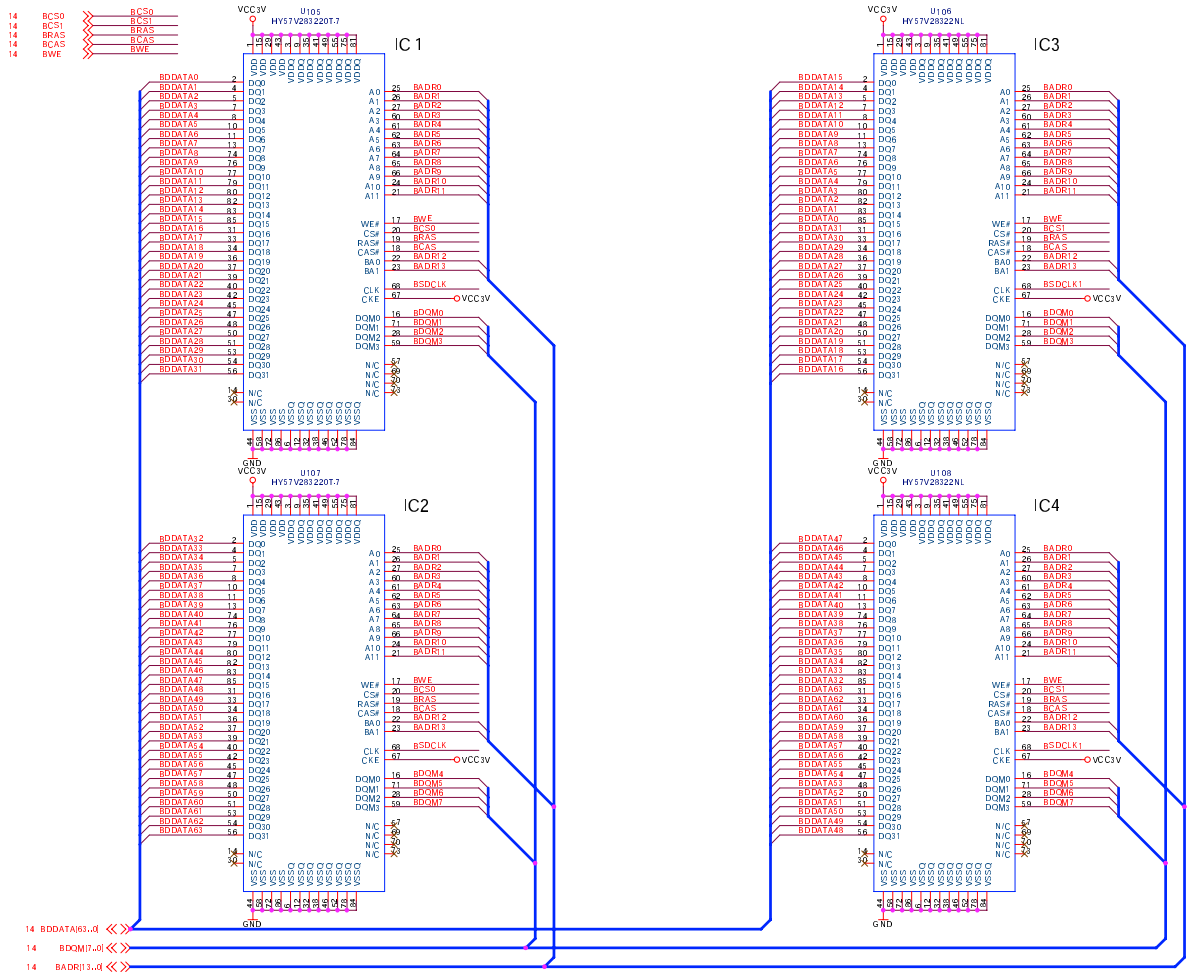
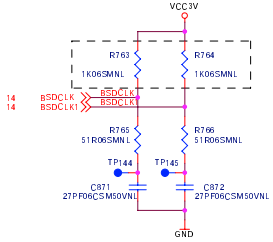
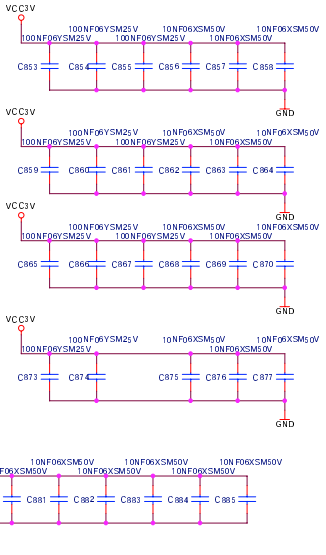


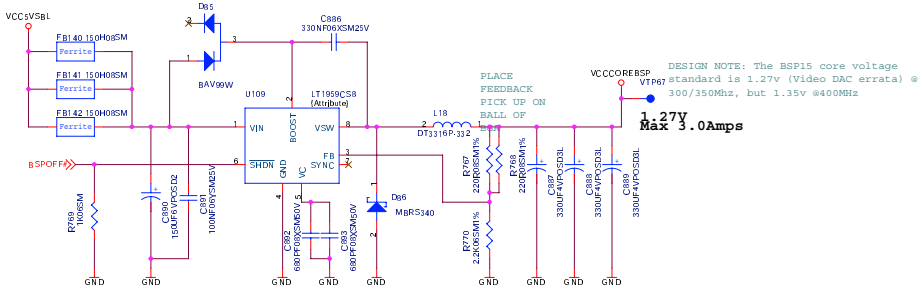
RESET STRAP	PULL UP	PULL DOWN
0	FLASH ROM BOOT	ROM LESS BOOT
1	PCI HOST	PCI SLAVE
4	SW CONFIGURABLE STRAP 0	
5	SW CONFIGURABLE STRAP 1	
6	SW CONFIGURABLE STRAP 2	
7	SW CONFIGURABLE STRAP 3	







DESIGN NOTE: Needs a really good copper heatsink



VALID MEMORY IC's

HYNIX HY57V283220T 4Banks X 1M X32bit 86TSOP-II
MICRON MT48LC4M32B2 4Banks X 1M X32bit 86TSOP-II
MICRON MT48LC8M32B2 4Banks X 2M X32bit 86TSOP-II

VALID ARRANGEMENTS

	IC 1	IC2	IC3	IC4
32MB 2 IC's	HY57V283220T OR MT48LC4M32B2	HY57V283220T OR MT48LC4M32B2	NL	NL
64MB 2 IC's	MT48LC8M32B2	MT48LC8M32B2	NL	NL
64MB 4 IC's	HY57V283220T OR MT48LC4M32B2	HY57V283220T OR MT48LC4M32B2	HY57V283220T OR MT48LC4M32B2	HY57V283220T OR MT48LC4M32B2
128MB 4 IC's	MT48LC8M32B2	MT48LC8M32B2	MT48LC8M32B2	MT48LC8M32B2

BSP MEMORY AND POWER

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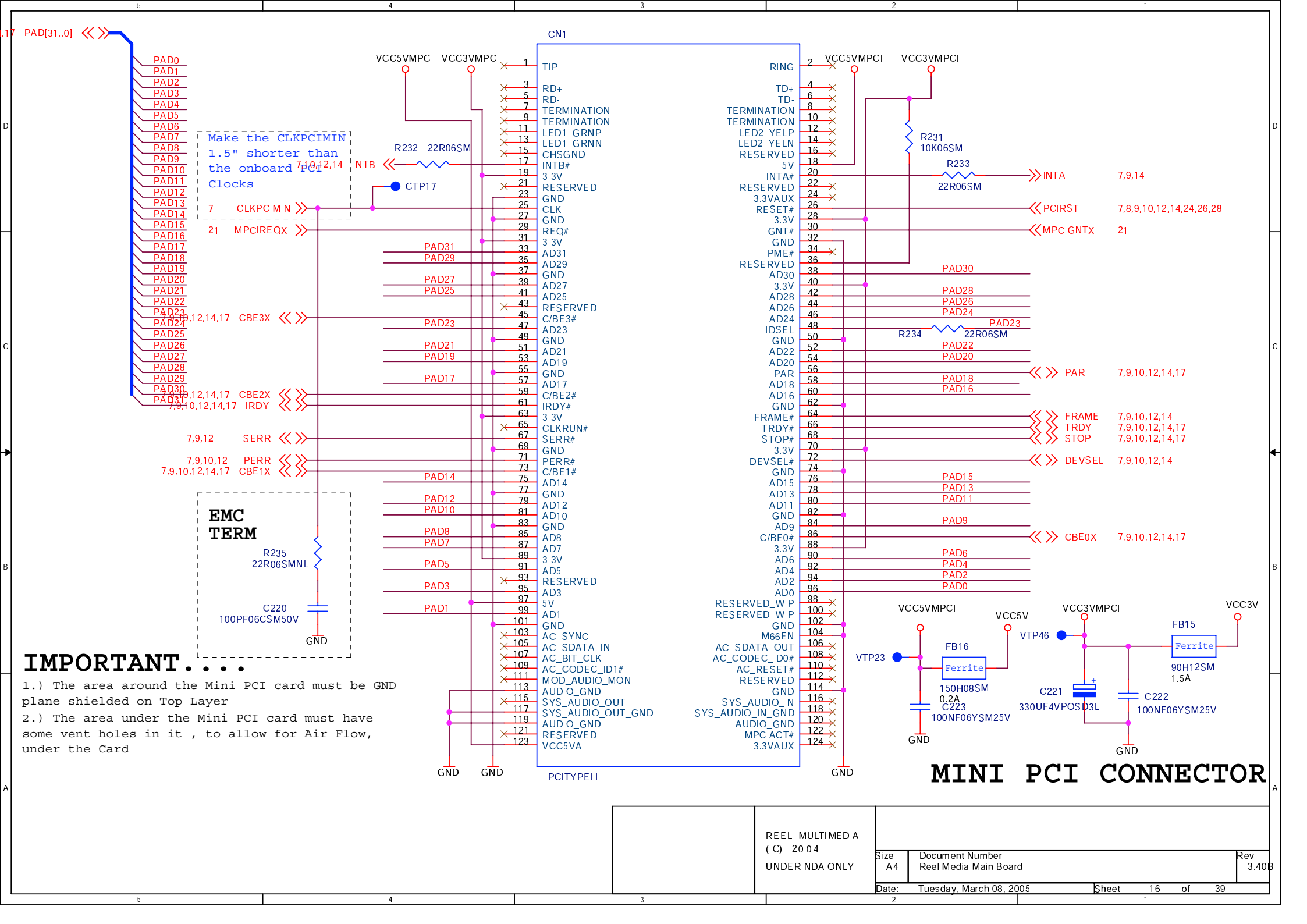

IMPORTANT....

1.) The area around the Mini PCI card must be GND plane shielded on Top Layer

2.) The area under the Mini PCI card must have some vent holes in it , to allow for Air Flow, under the Card

MINI PCI CONNECTOR

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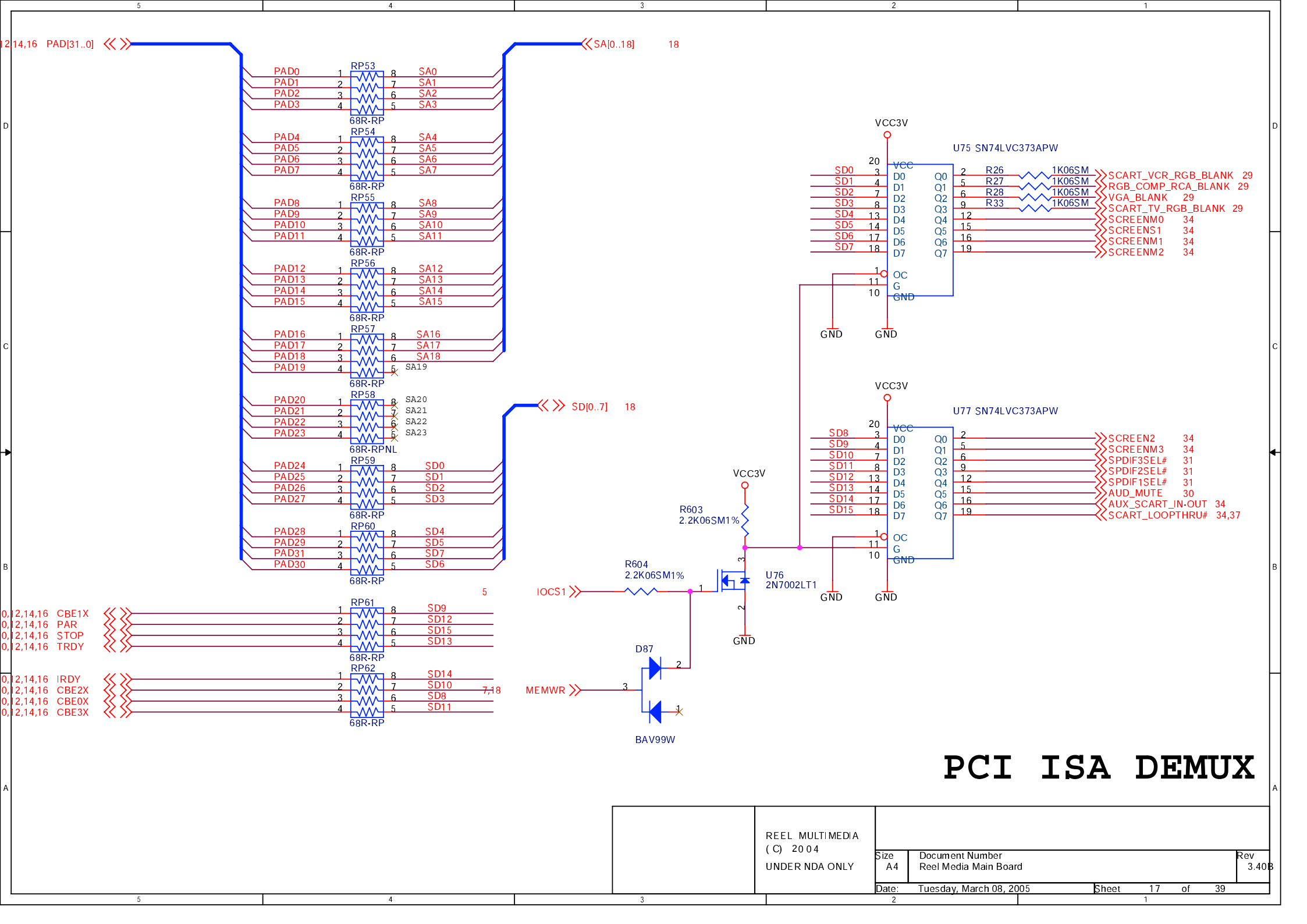

PCI ISA DEMUX

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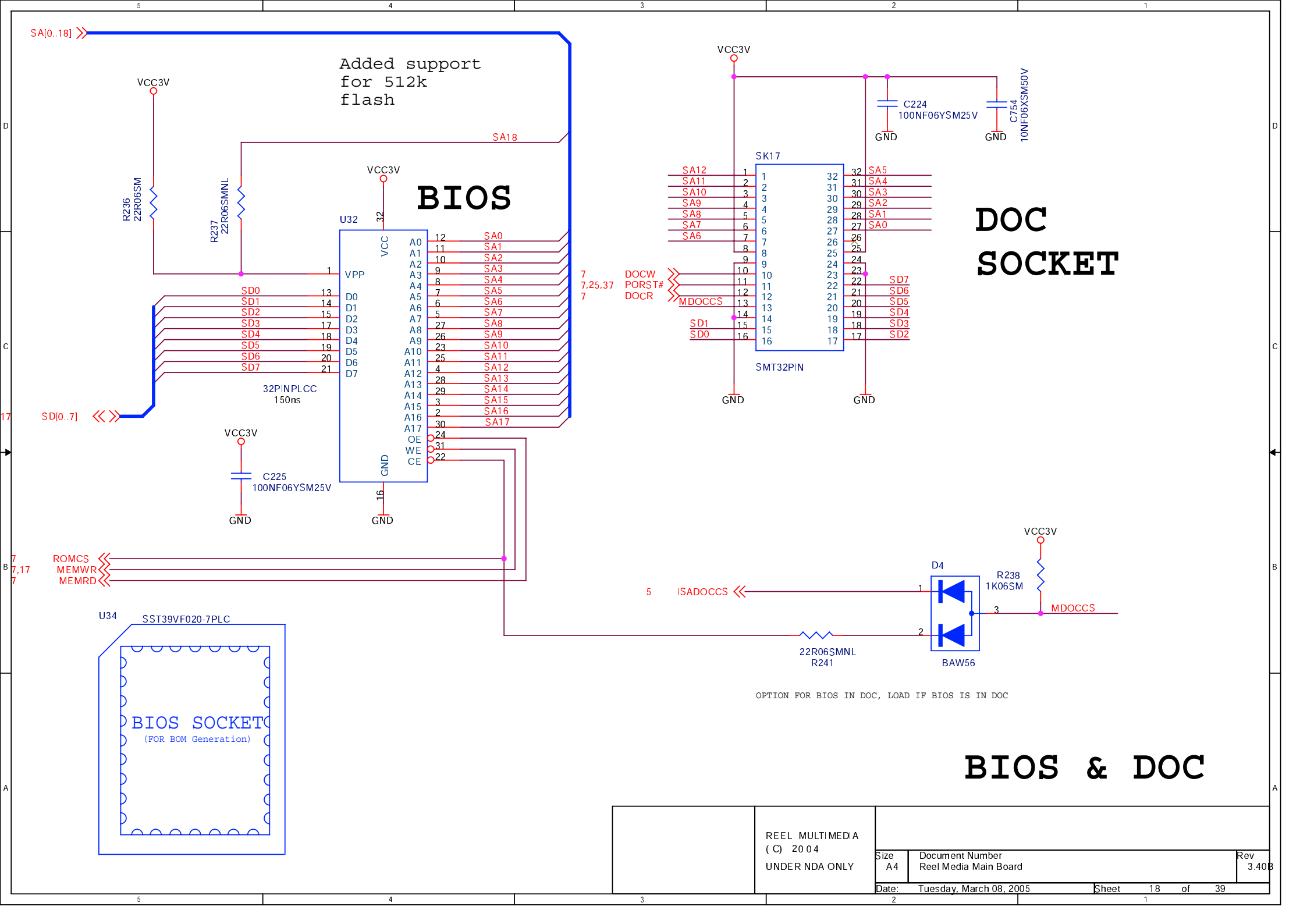
SA[0..18]
Added support for 512k flash
BIOS
VCC3V
R236 22R06SM
R237 22R06SMNL
SA18
U32
VPP
VCC
GND
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD[0..7]
32PINPLCC
150ns
C225
100NF06YSM25V
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
OE
WE
CE
DOCW
PORST#
DOCR
MDOCCS
SK17
SMT32PIN
C224
100NF06YSM25V
C754
10NF06XSM50V
DOC SOCKET
ROMCS
MEMWR
MEMRD
ISADOCCS
D4
BAW56
R238
1K06SM
22R06SMNL
R241
U34
SST39VF020-7PLC
BIOS SOCKET
(FOR BOM Generation)
OPTION FOR BIOS IN DOC, LOAD IF BIOS IS IN DOC
BIOS & DOC
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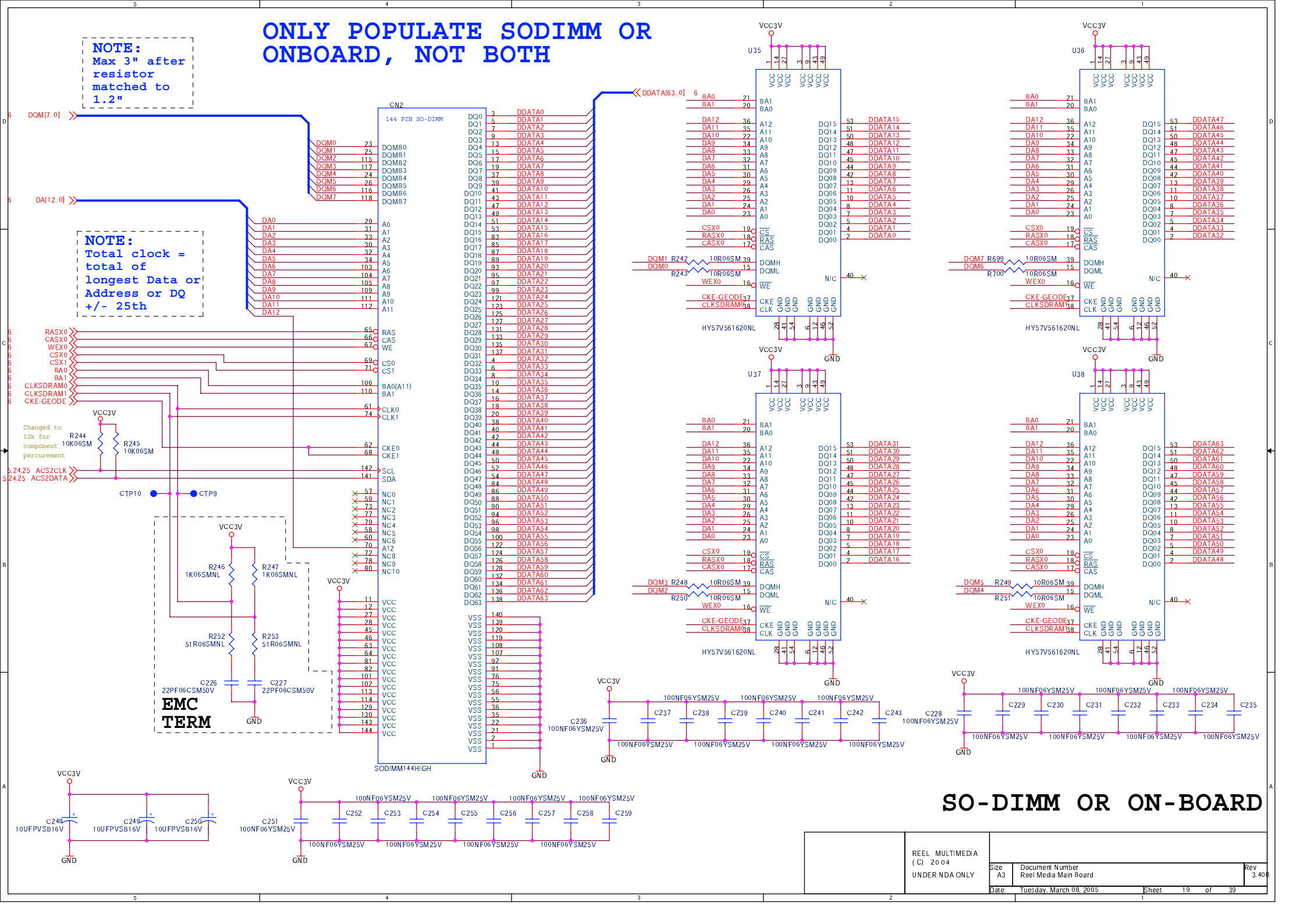
ONLY POPULATE SODIMM OR ONBOARD, NOT BOTH

NOTE:
Max 3" after resistor matched to 1.2"

NOTE:
Total clock = total of longest Data or Address or DQ +/- 25th



SO-DIMM OR ON-BOARD

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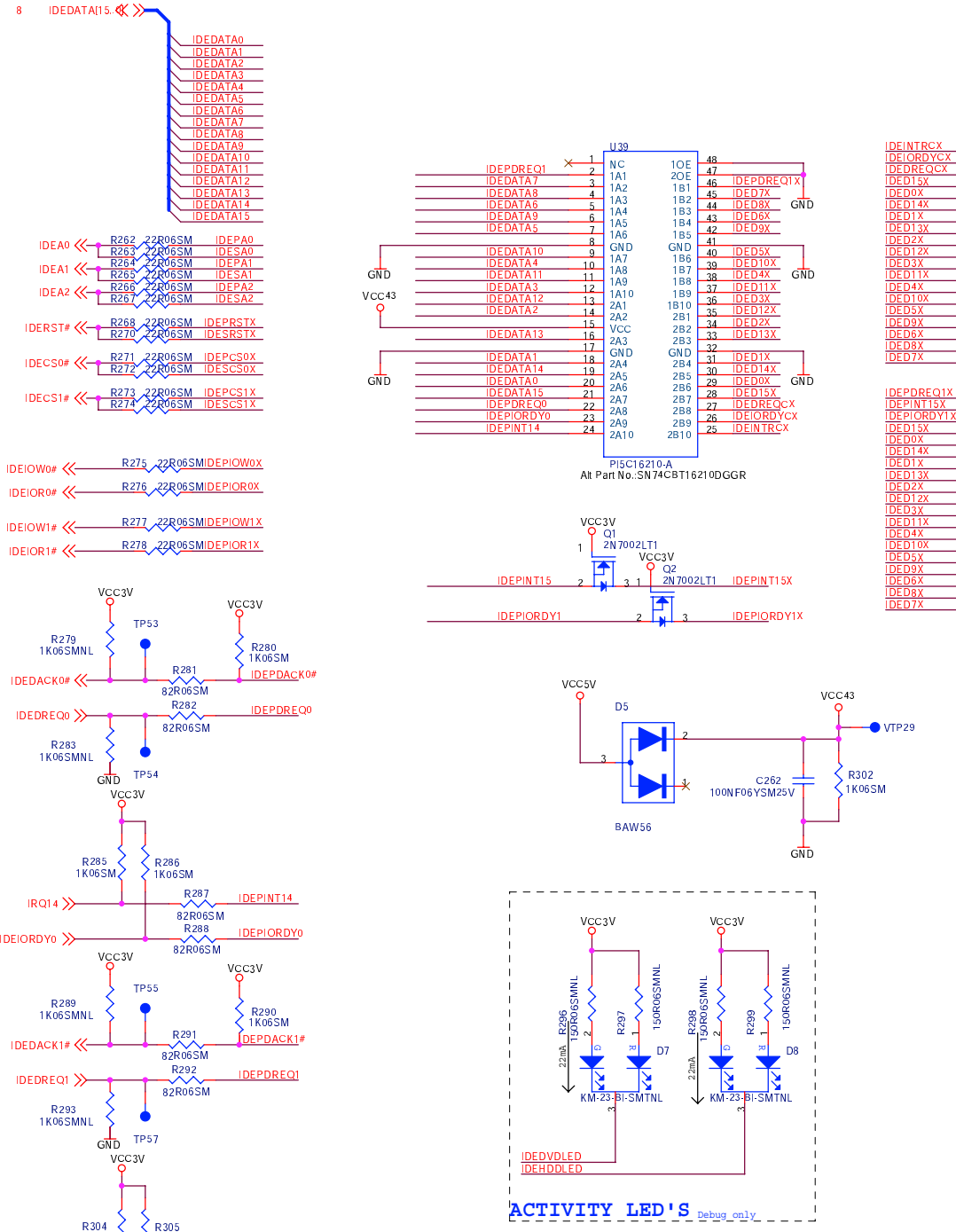
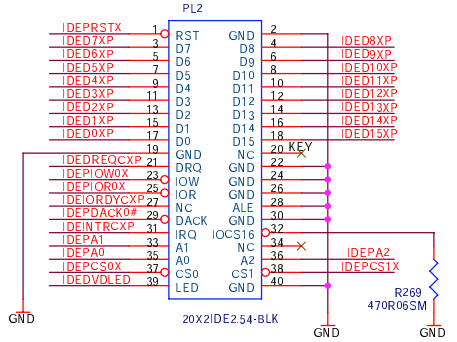
IDE CHANNEL 0

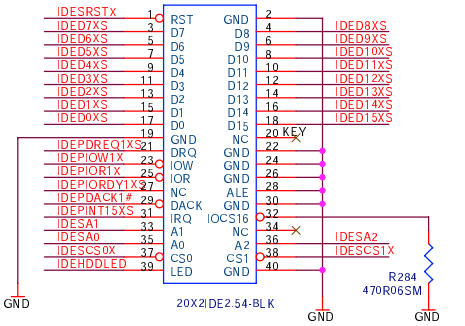
IDE CHANNEL 1



IDE (DVD) HEADER



IDE (HDD) HEADER



IDE CONNECTORS

	REEL MULTIMEDIA (C) 2004 UNDER NDA ONLY		
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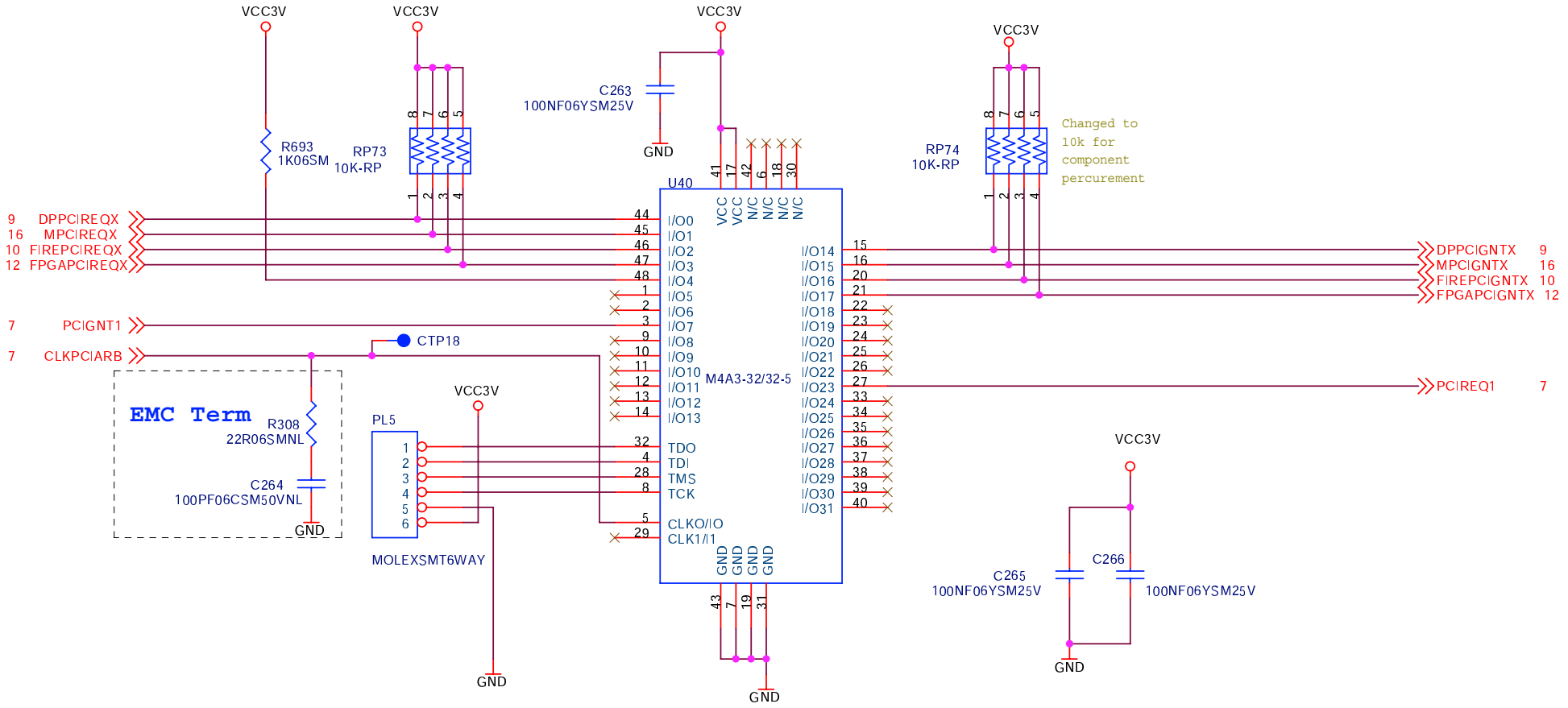

ARBITOR

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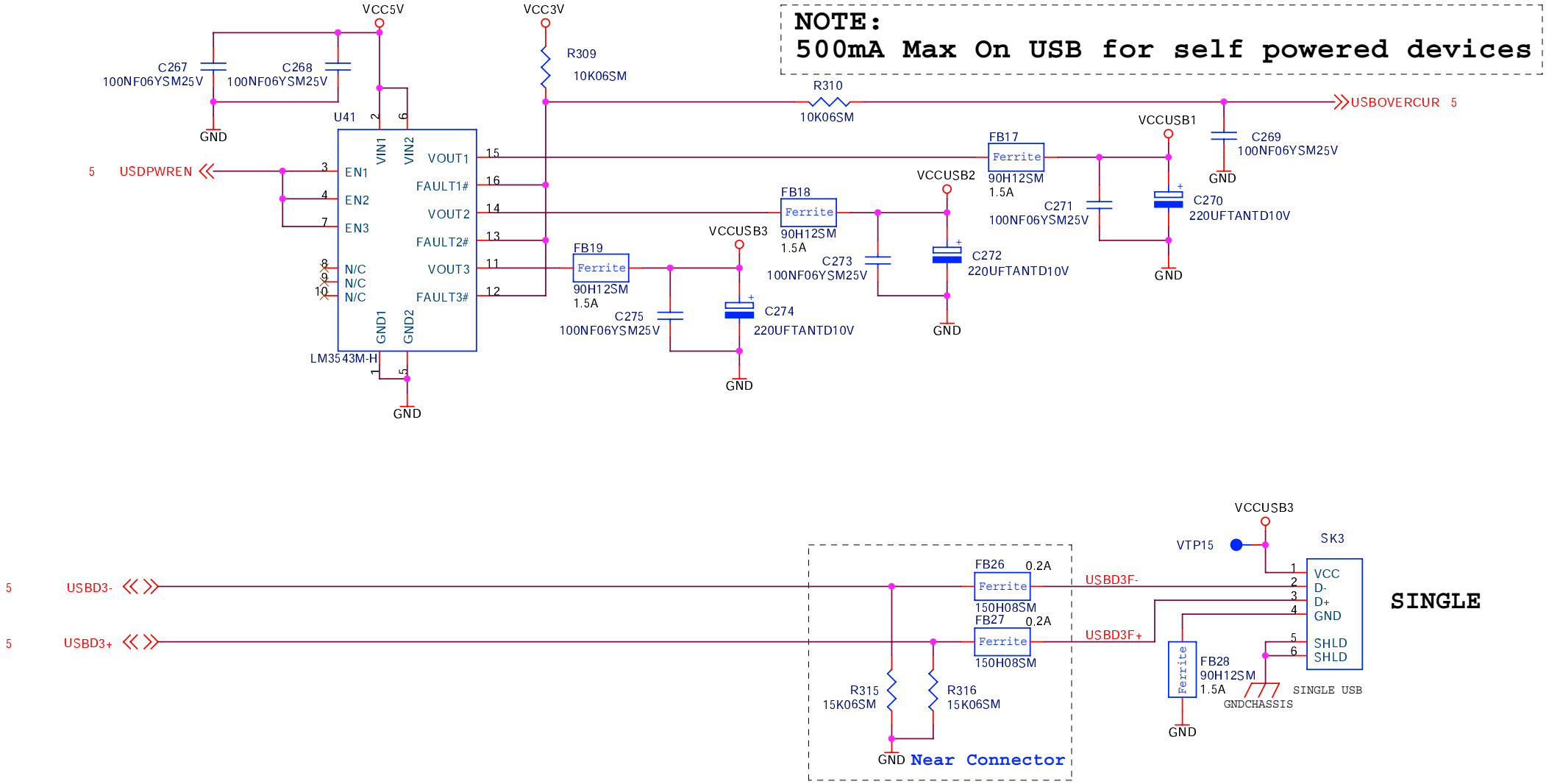

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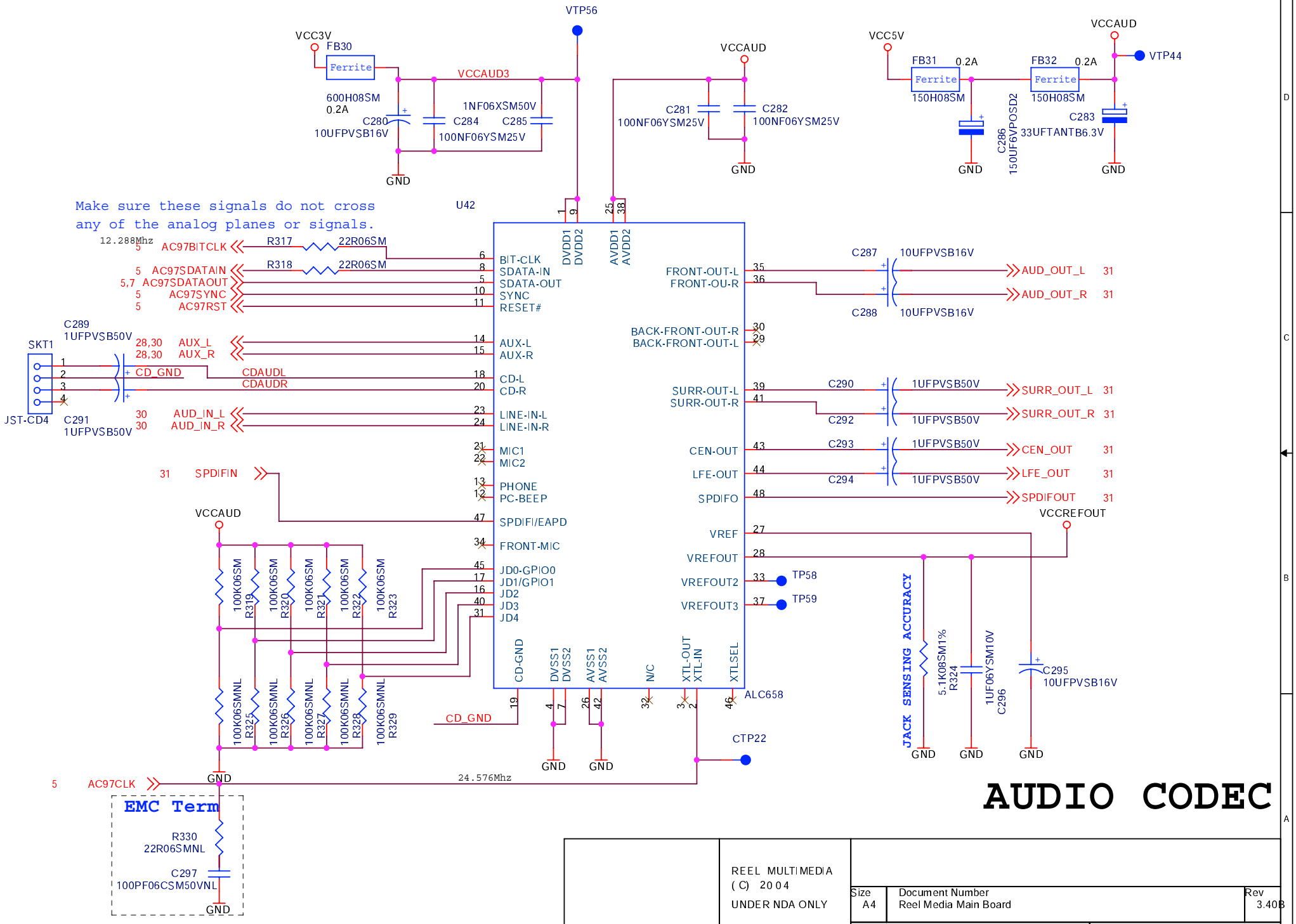
VTP56
VCC3V
FB30
Ferrite
600H08SM
0.2A
VCCAUD3
C280
10UFPVSB16V
C284
100NF06YSM25V
C285
1NF06XSM50V
GND
VCCAUD
C281
100NF06YSM25V
C282
100NF06YSM25V
GND
VCC5V
FB31
0.2A
Ferrite
150H08SM
GND
C286
150UF6VPOSD2
FB32
0.2A
Ferrite
150H08SM
C283
33UFTANTB6.3V
GND
VCCAUD
VTP44
Make sure these signals do not cross
any of the analog planes or signals.
U42
DVDD1
DVDD2
AVDD1
AVDD2
12.288Mhz
5 AC97BITCLK
R317
22R06SM
5 AC97SDATAIN
R318
22R06SM
5,7 AC97SDATAOUT
5 AC97SYNC
5 AC97RST
BIT-CLK
SDATA-IN
SDATA-OUT
SYNC
RESET#
C289
1UFPVSB50V
SKT1
28,30 AUX_L
28,30 AUX_R
CD_GND
CDAUDL
CDAUDR
JST-CD4
C291
1UFPVSB50V
AUX-L
AUX-R
CD-L
CD-R
30 AUD_IN_L
30 AUD_IN_R
LINE-IN-L
LINE-IN-R
MIC1
MIC2
PHONE
PC-BEEP
31 SPDIFIN
SPDIFI/EAPD
FRONT-MIC
JD0-GPIO0
JD1/GPIO1
JD2
JD3
JD4
FRONT-OUT-L
FRONT-OU-R
C287
10UFPVSB16V
C288
10UFPVSB16V
AUD_OUT_L 31
AUD_OUT_R 31
BACK-FRONT-OUT-R
BACK-FRONT-OUT-L
SURR-OUT-L
SURR-OUT-R
C290
1UFPVSB50V
C292
1UFPVSB50V
SURR_OUT_L 31
SURR_OUT_R 31
CEN-OUT
LFE-OUT
C293
1UFPVSB50V
C294
1UFPVSB50V
CEN_OUT 31
LFE_OUT 31
SPDIFO
SPDIFOUT 31
VCCREFOUT
VREF
VREFOUT
VREFOUT2
VREFOUT3
TP58
TP59
VCCAUD
100K06SM R319
100K06SM R320
100K06SM R321
100K06SM R322
100K06SM R323
100K06SMNL R325
100K06SMNL R326
100K06SMNL R327
100K06SMNL R328
100K06SMNL R329
CD-GND
DVSS1
DVSS2
AVSS1
AVSS2
N/C
XTL-OUT
XTL-IN
XTLSEL
ALC658
CD_GND
CTP22
GND
JACK SENSING ACCURACY
5.1K08SM1%
R324
1UF06YSM10V
C296
C295
10UFPVSB16V
5 AC97CLK
24.576Mhz
EMC Term
R330
22R06SMNL
C297
100PF06CSM50VNL
AUDIO CODEC
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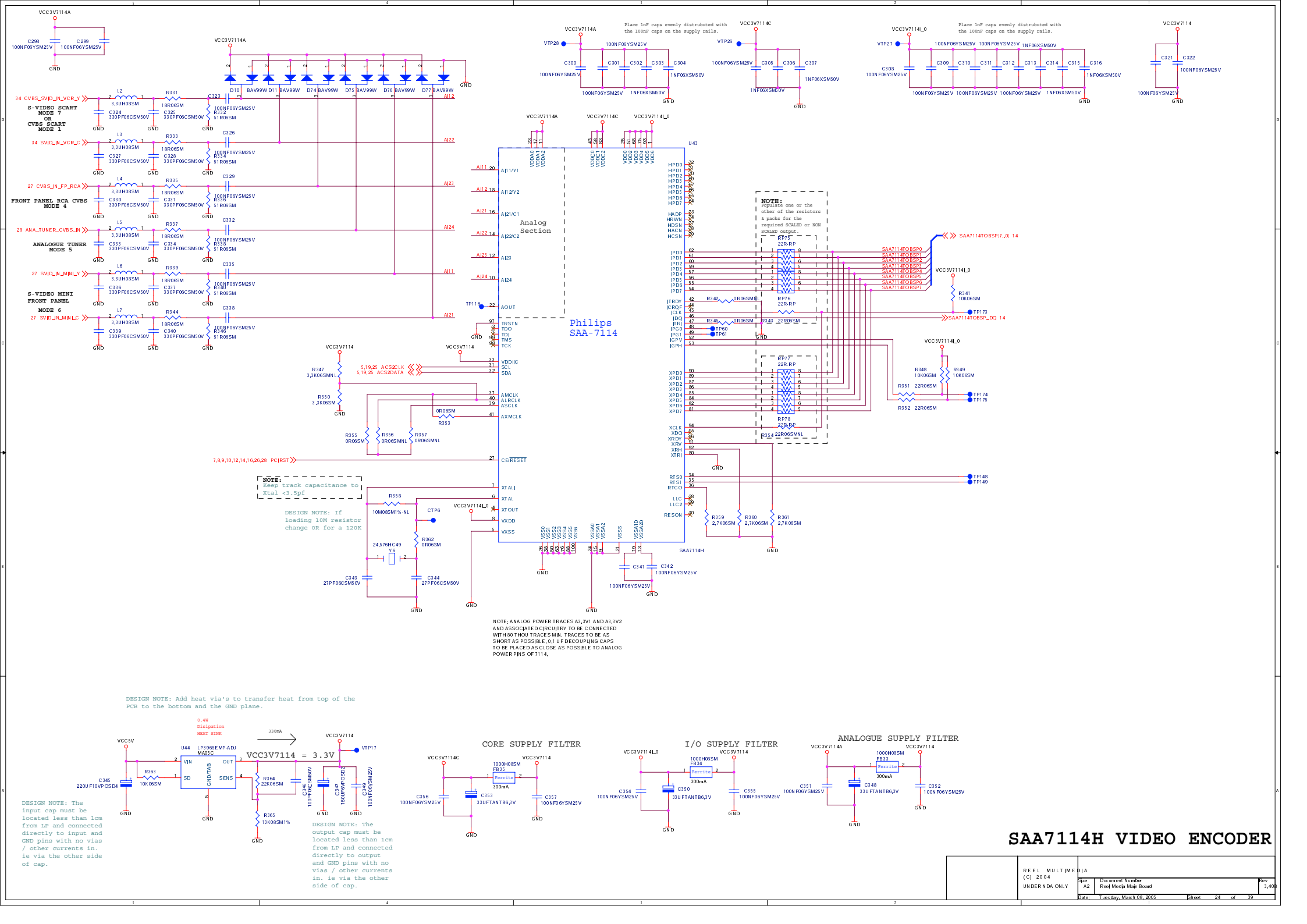
S-VIDEO SCART MODE 7 OR CVBS SCART MODE 1
FRONT PANEL RCA CVBS MODE 4
ANALOGUE TUNER MODE 5
S-VIDEO MINI FRONT PANEL MODE 6
Analog Section
Philips SAA-7114
SAA7114H
NOTE: Populate one or the other of the resistors & packs for the required SCALED or NON SCALED output.
NOTE: Keep track capacitance to Xtal <3.5pf
DESIGN NOTE: If loading 10M resistor change 0R for a 120K
NOTE: ANALOG POWER TRACES A3,3V1 AND A3,3V2 AND ASSOCIATED CIRCUITRY TO BE CONNECTED WITH 80 THOU TRACES MIN. TRACES TO BE AS SHORT AS POSSIBLE, 0,1 UF DECOUPLING CAPS TO BE PLACED AS CLOSE AS POSSIBLE TO ANALOG POWER PINS OF 7114,
DESIGN NOTE: Add heat via's to transfer heat from top of the PCB to the bottom and the GND plane.
VCC3V7114 = 3.3V
DESIGN NOTE: The input cap must be located less than 1cm from LP and connected directly to input and GND pins with no vias / other currents in. ie via the other side of cap.
DESIGN NOTE: The output cap must be located less than 1cm from LP and connected directly to output and GND pins with no vias / other currents in. ie via the other side of cap.
CORE SUPPLY FILTER
I/O SUPPLY FILTER
ANALOGUE SUPPLY FILTER
SAA7114H VIDEO ENCODER
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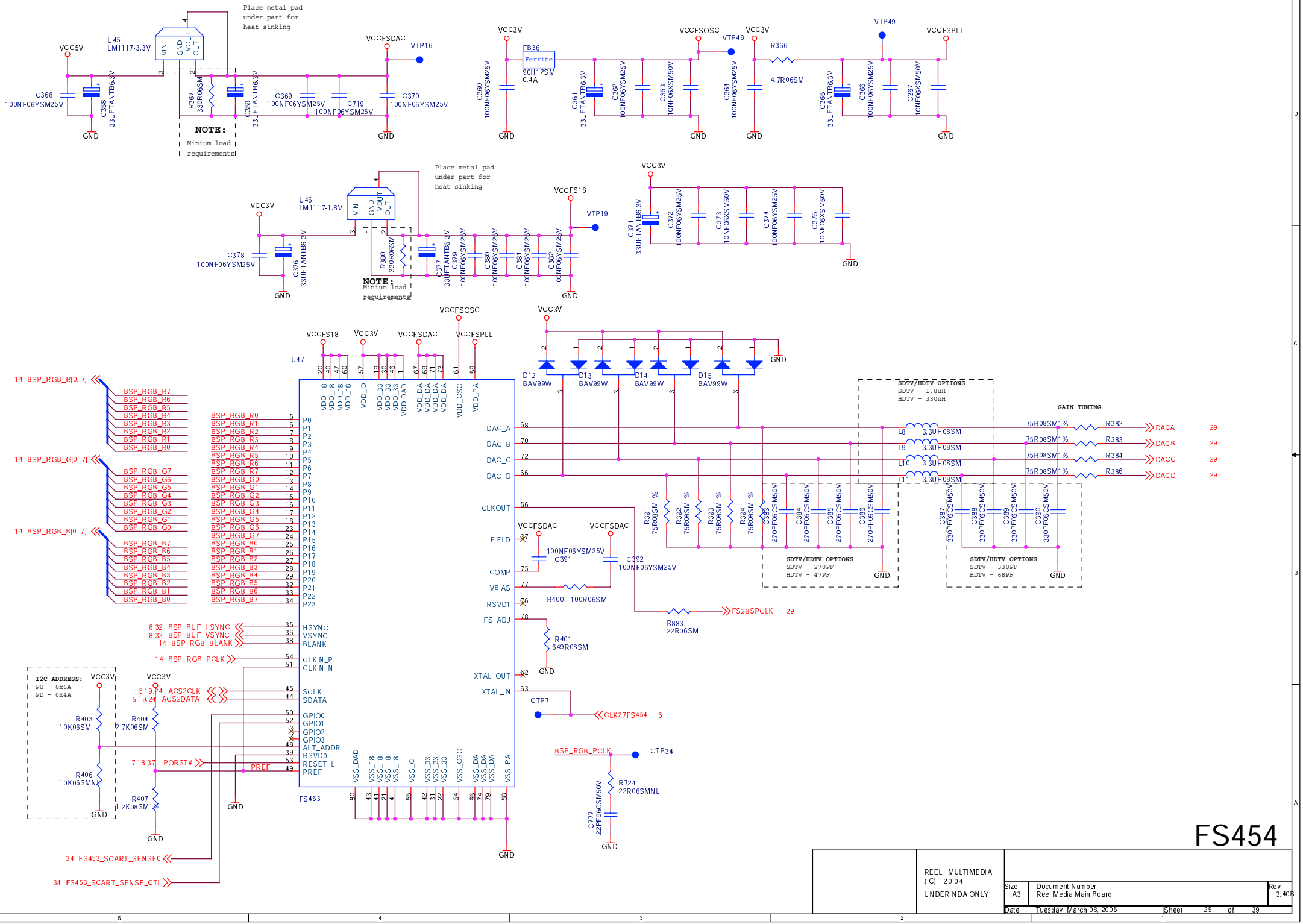
Place metal pad under part for heat sinking
U45 LM1117-3.3V
VIN GND VOUT OUT
VCC5V
VCCFSDAC
VTP16
C368 100NF06YSM25V
C358 33UFTANTB6.3V
R367 330R06SM
C359 33UFTANTB6.3V
C369 100NF06YSM25V
C719 100NF06YSM25V
C370 100NF06YSM25V
NOTE:
Minium load requirements
GND
VCC3V
FB36 Ferrite 90H12SM 0.4A
VCCFSOSC
VTP48
VTP49
VCCFSPLL
R366 4.7R06SM
C360 100NF06YSM25V
C361 33UFTANTB6.3V
C362 100NF06YSM25V
C363 10NF06XSM50V
C364 100NF06YSM25V
C365 33UFTANTB6.3V
C366 100NF06YSM25V
C367 10NF06XSM50V
U46 LM1117-1.8V
VTP19
VCCFS18
C378 100NF06YSM25V
C376 33UFTANTB6.3V
R380 330R06SM
C377 33UFTANTB6.3V
C379 100NF06YSM25V
C380 100NF06YSM25V
C381 100NF06YSM25V
C382 100NF06YSM25V
C371 33UFTANTB6.3V
C372 100NF06YSM25V
C373 10NF06XSM50V
C374 100NF06YSM25V
C375 10NF06XSM50V
U47
VCCFS18 VCC3V VCCFSDAC VCCFSOSC VCCFSPLL
D12 BAV99W
D13 BAV99W
D14 BAV99W
D15 BAV99W
SDTV/HDTV OPTIONS
SDTV = 1.8uH
HDTV = 330nH
GAIN TUNING
L8 3.3UH08SM
L9 3.3UH08SM
L10 3.3UH08SM
L11 3.3UH08SM
75R08SM1% R382 DACA 29
75R08SM1% R383 DACB 29
75R08SM1% R384 DACC 29
75R08SM1% R386 DACD 29
14 BSP_RGB_R[0..7]
14 BSP_RGB_G[0..7]
14 BSP_RGB_B[0..7]
BSP_RGB_R0 BSP_RGB_R1 BSP_RGB_R2 BSP_RGB_R3 BSP_RGB_R4 BSP_RGB_R5 BSP_RGB_R6 BSP_RGB_R7
BSP_RGB_G0 BSP_RGB_G1 BSP_RGB_G2 BSP_RGB_G3 BSP_RGB_G4 BSP_RGB_G5 BSP_RGB_G6 BSP_RGB_G7
BSP_RGB_B0 BSP_RGB_B1 BSP_RGB_B2 BSP_RGB_B3 BSP_RGB_B4 BSP_RGB_B5 BSP_RGB_B6 BSP_RGB_B7
DAC_A DAC_B DAC_C DAC_D
CLKOUT FIELD COMP VBIAS RSVD1 FS_ADJ XTAL_OUT XTAL_IN
R391 75R08SM1% R392 75R08SM1% R393 75R08SM1% R394 75R08SM1%
C383 270PF06CSM50V C384 270PF06CSM50V C385 270PF06CSM50V C386 270PF06CSM50V
C387 330PF06CSM50V C388 330PF06CSM50V C389 330PF06CSM50V C390 330PF06CSM50V
SDTV/HDTV OPTIONS
SDTV = 270PF
HDTV = 47PF
SDTV/HDTV OPTIONS
SDTV = 330PF
HDTV = 68PF
C391 100NF06YSM25V
C392 100NF06YSM25V
R400 100R06SM
R883 22R06SM
FS2BSPCLK 29
R401 649R08SM
CTP7
CLK27FS454 6
8,32 BSP_BUF_HSYNC
8,32 BSP_BUF_VSYNC
14 BSP_RGB_BLANK
14 BSP_RGB_PCLK
HSYNC VSYNC BLANK CLKIN_P CLKIN_N
I2C ADDRESS:
PU = 0x6A
PD = 0x4A
R403 10K06SM
R404 2.7K06SM
R406 10K06SMNL
R407 1.2K08SM1%
5,19,24 ACS2CLK
5,19,24 ACS2DATA
7,18,37 PORST#
PREF
SCLK SDATA GPIO0 GPIO1 GPIO2 GPIO3 ALT_ADDR RSVD0 RESET_L PREF
FS453
BSP_RGB_PCLK
CTP34
R724 22R06SMNL
C777 22PF06CSM50V
34 FS453_SCART_SENSE0
34 FS453_SCART_SENSE_CTL
FS454
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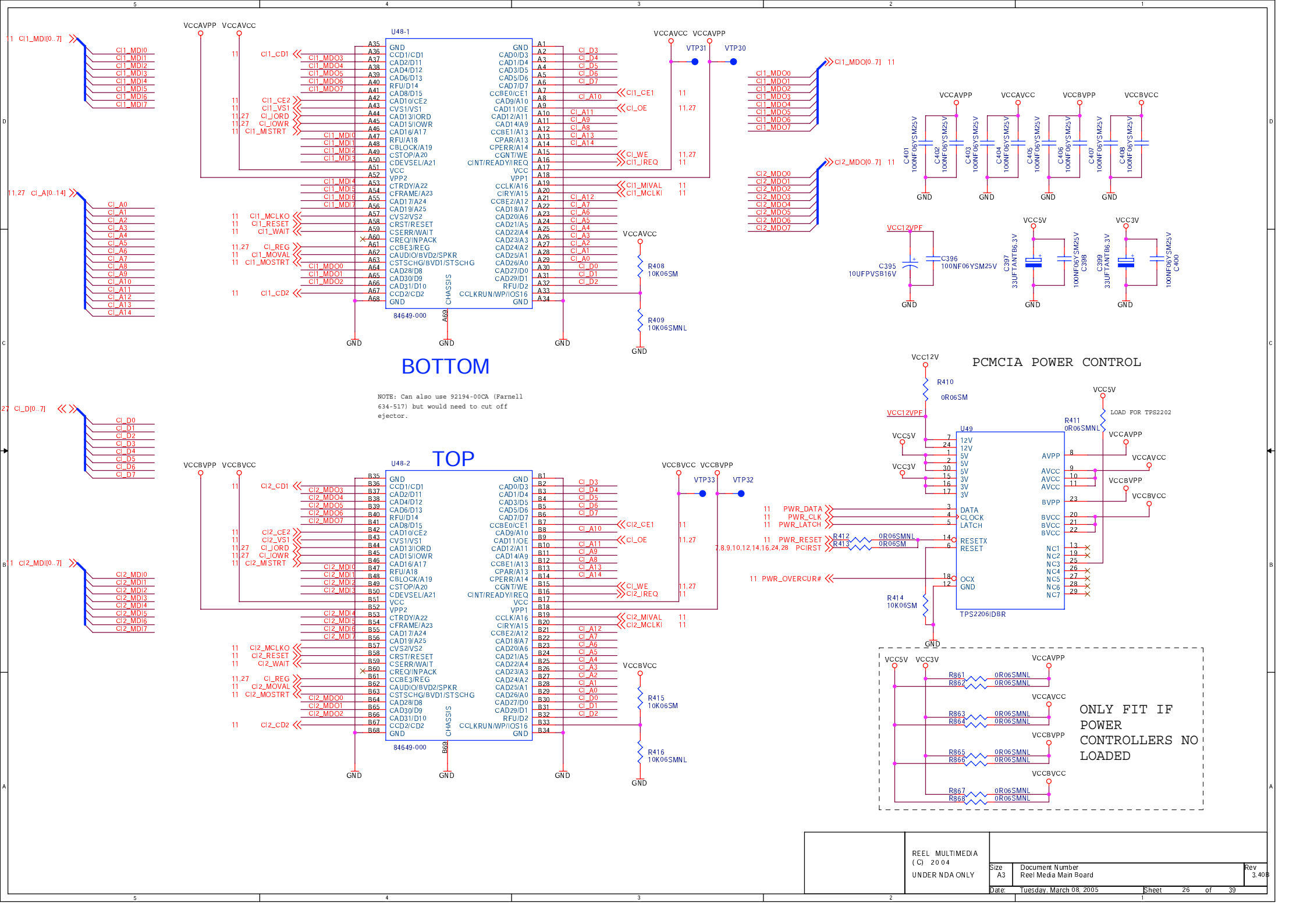
BOTTOM
TOP
NOTE: Can also use 92194-00CA (Farnell 634-517) but would need to cut off ejector.
PCMCIA POWER CONTROL
ONLY FIT IF POWER CONTROLLERS NO LOADED
TPS2206IDBR
84649-000
LOAD FOR TPS2202
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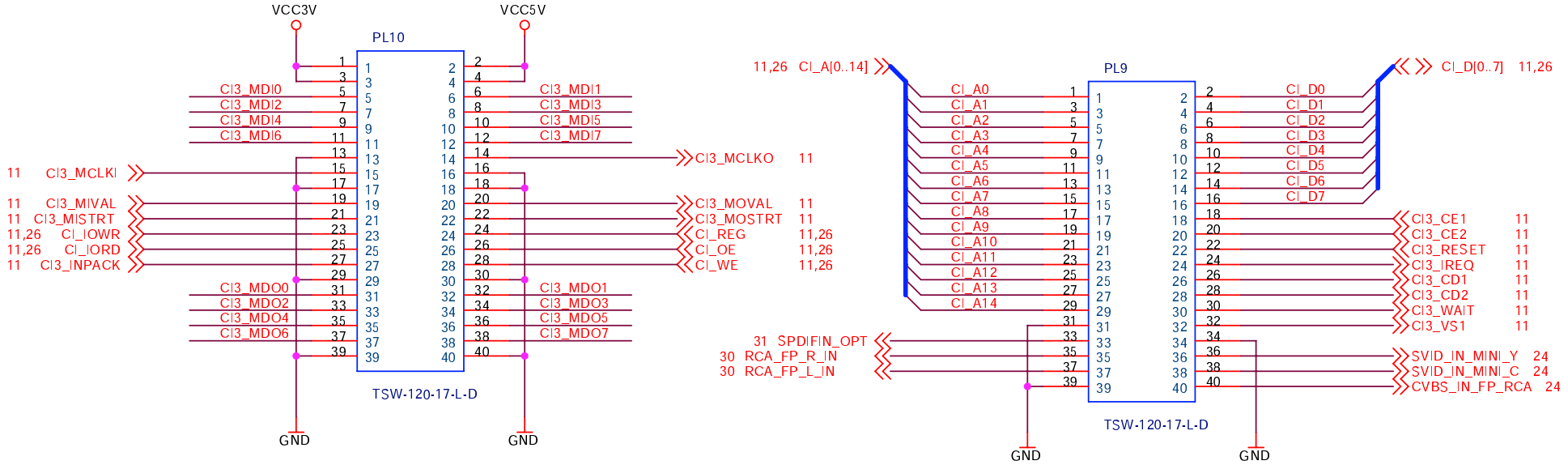

NEOTION CONNECTION

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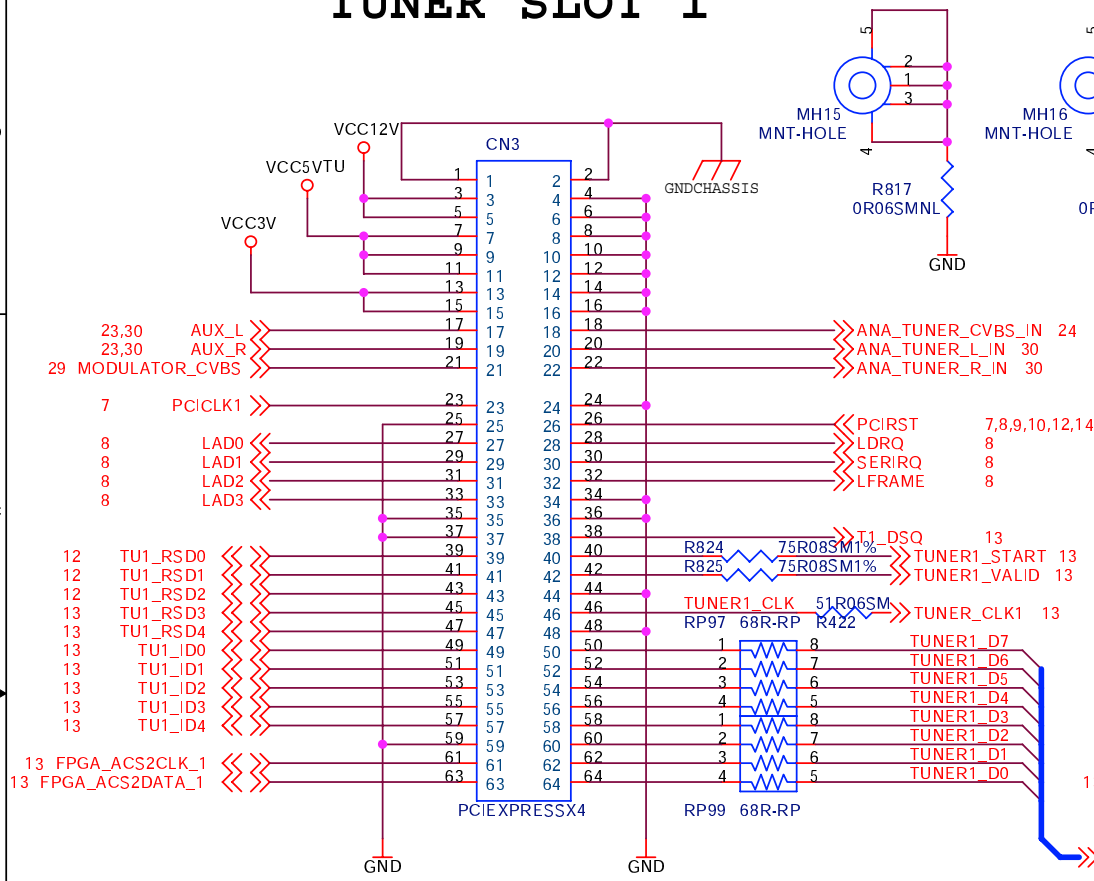
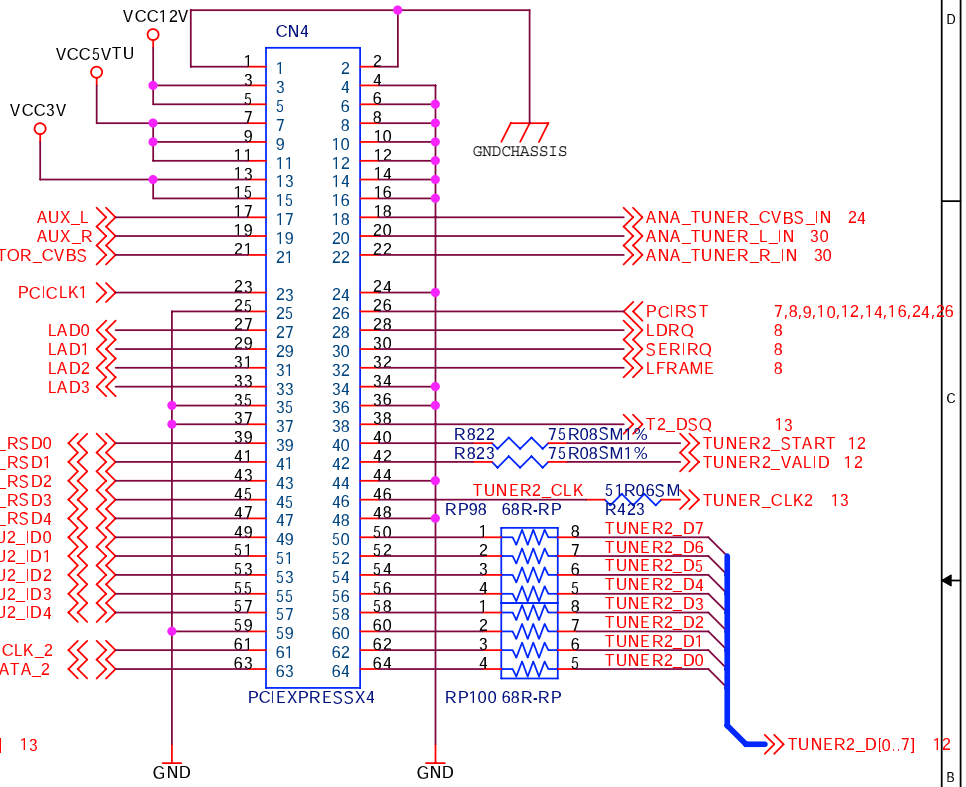
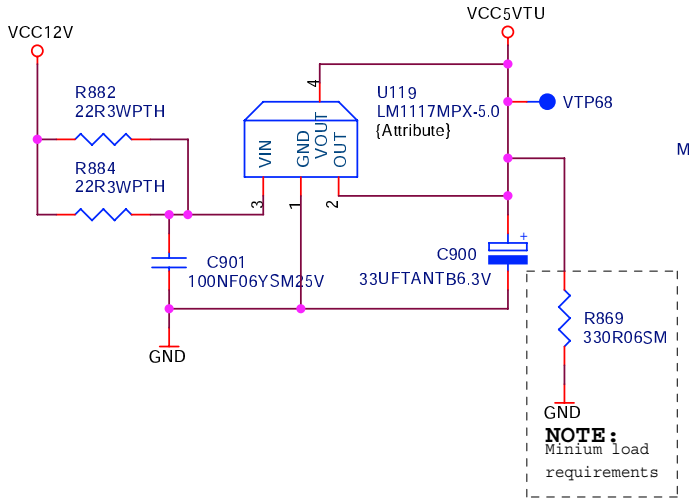
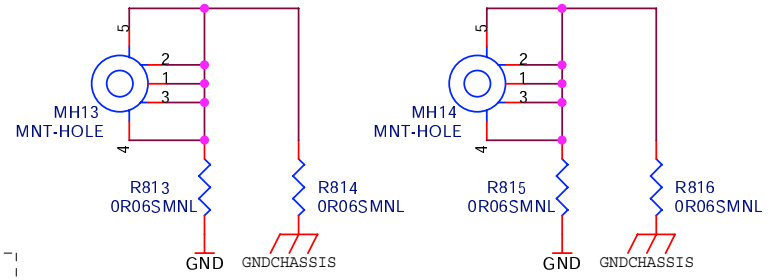
TUNER SLOT 1

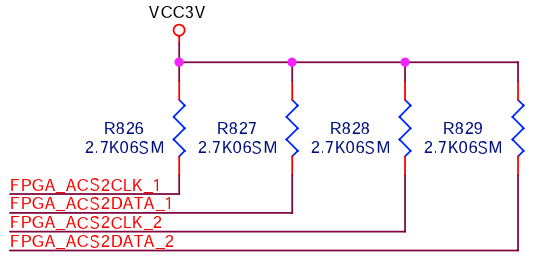


TUNER SLOT 2









TUNERS

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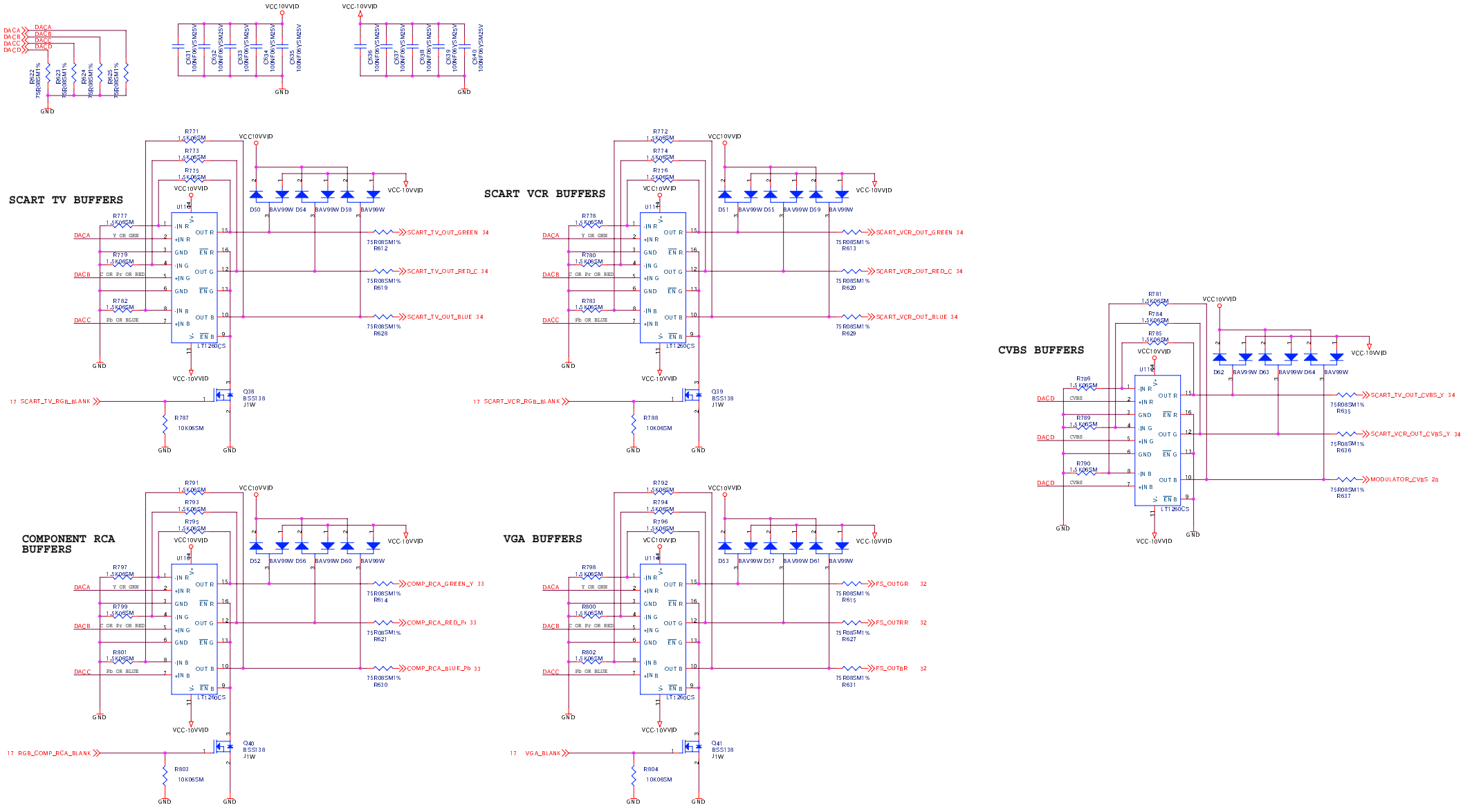

We have to switch the outputs. Because we could end up with a situation, where we are sending out an illegal signal on a connecor. IE component video onto SCART

VIDEO ROUTING

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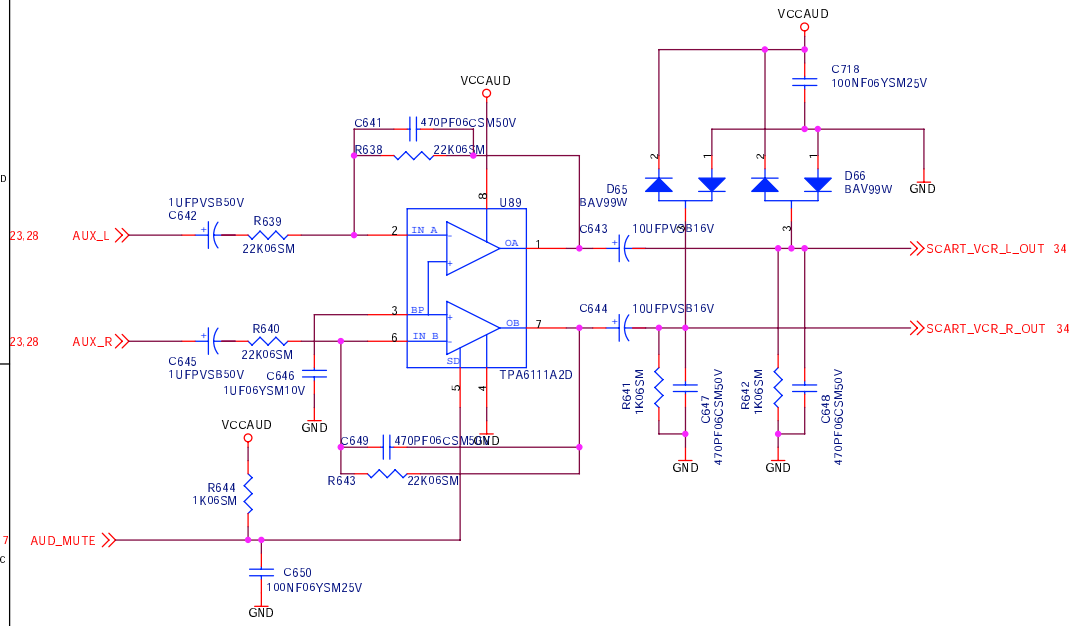

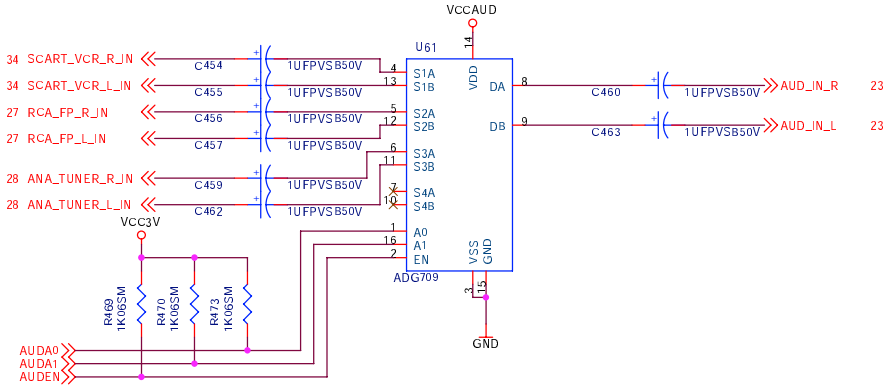

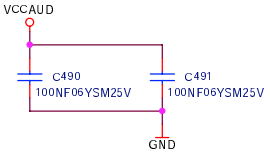

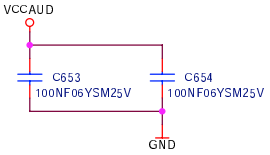

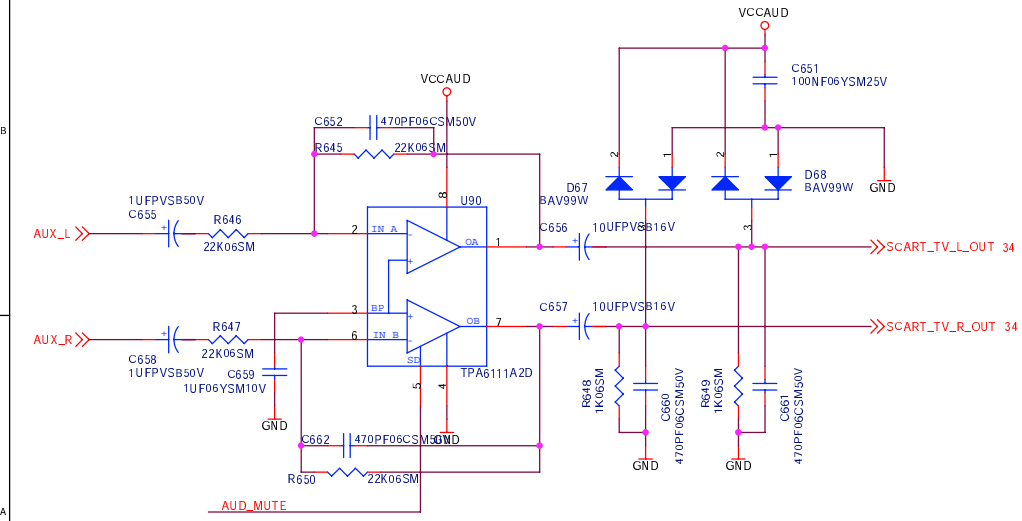

AUDIO ROUTING

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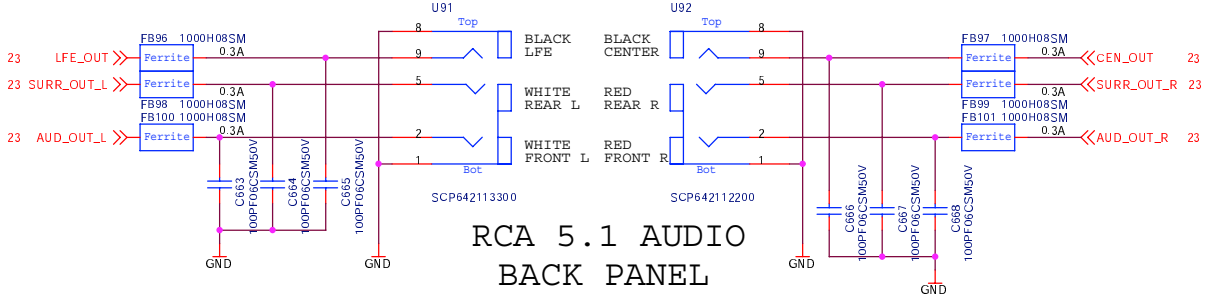
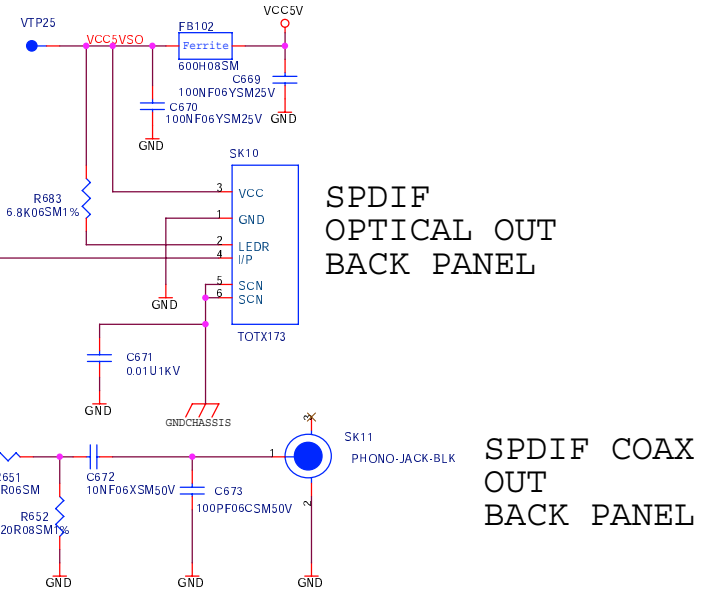


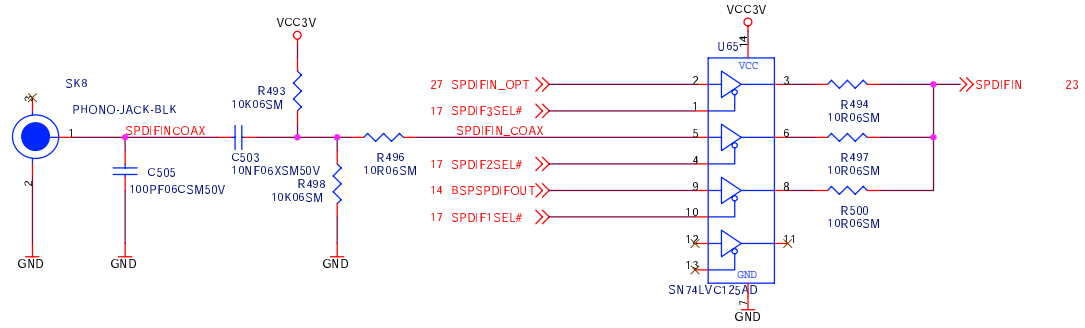
RCA 5.1 AUDIO
BACK PANEL

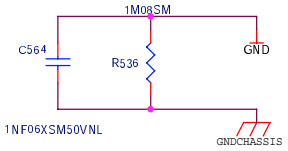


SPDIF
OPTICAL OUT
BACK PANEL

SPDIF COAX
OUT
BACK PANEL

SPDIF
COAX
IN
FRONT PANEL





5.1 AND SPDIF

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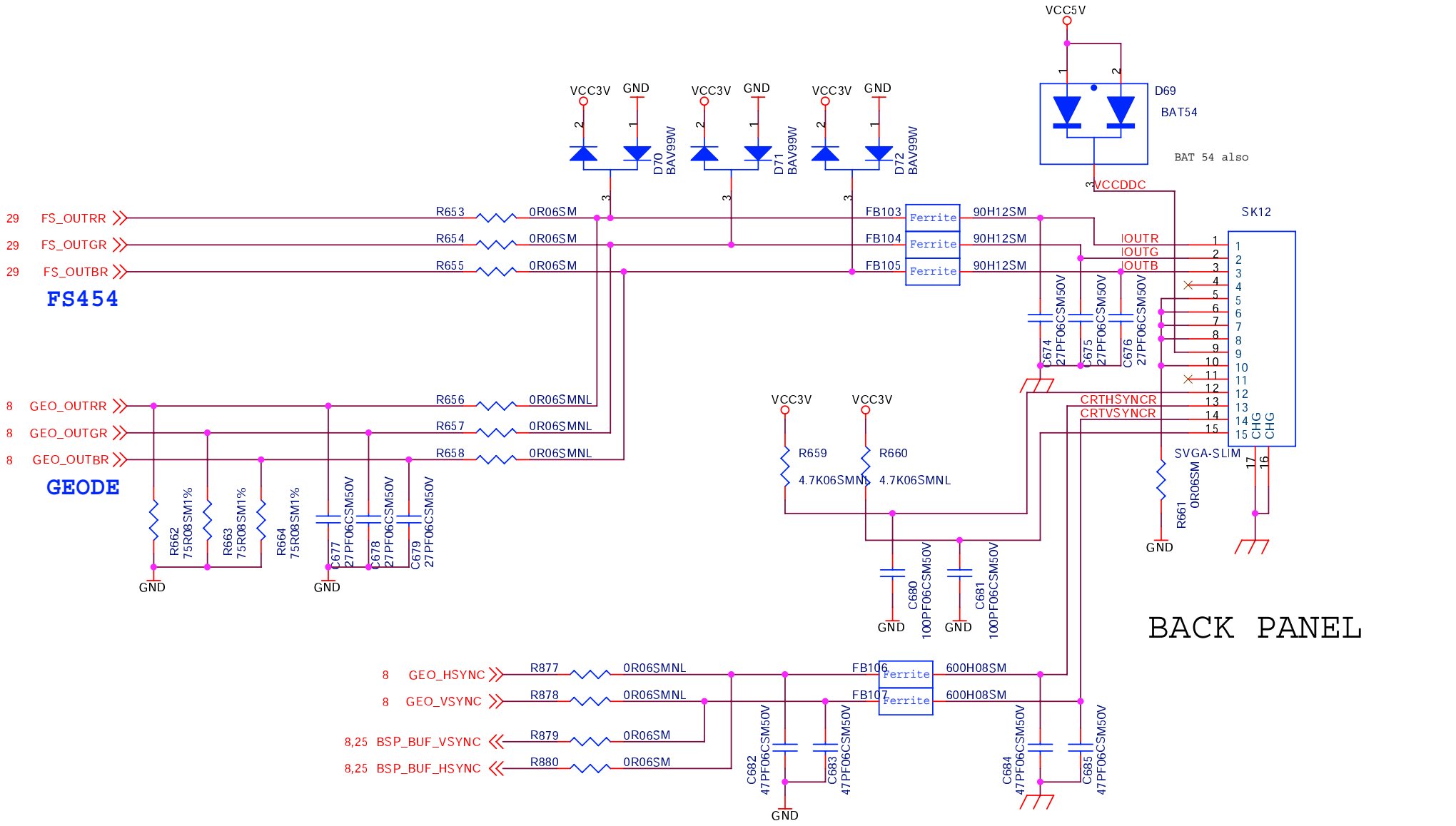

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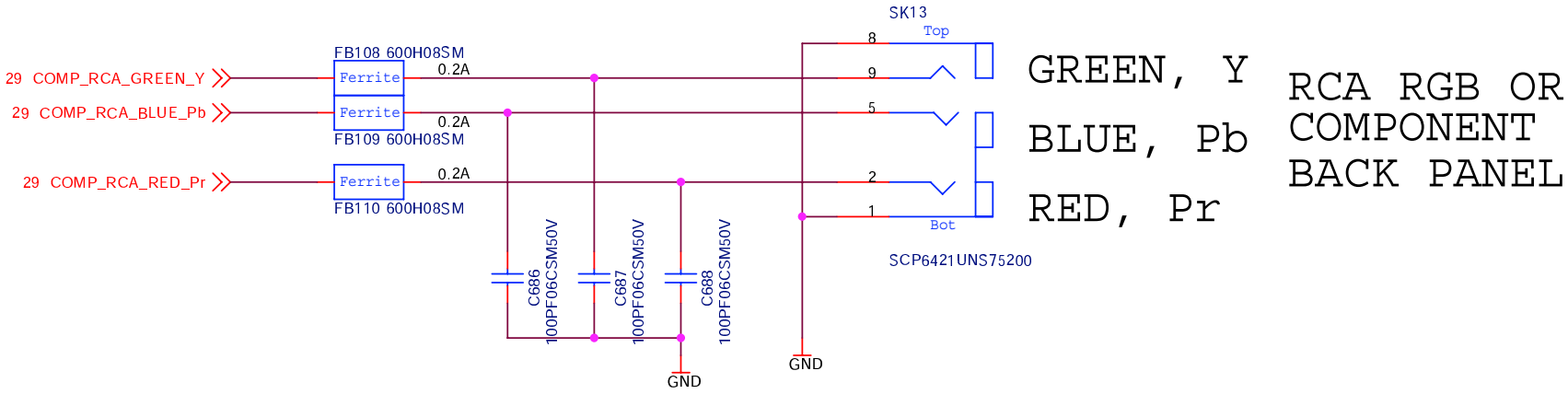

RGB AND COMPONENT

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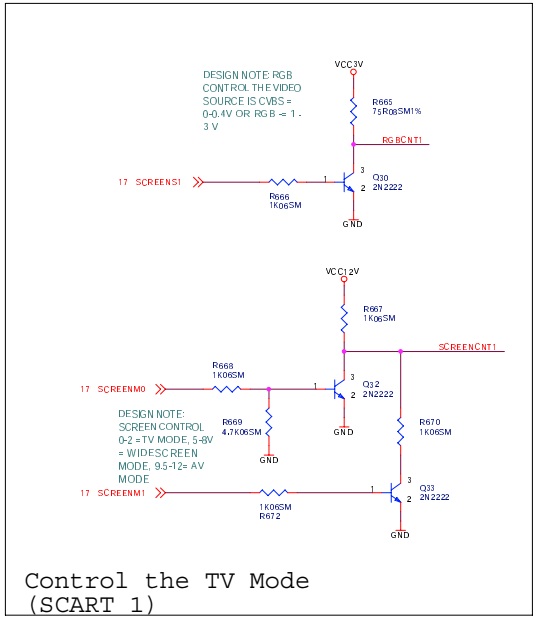
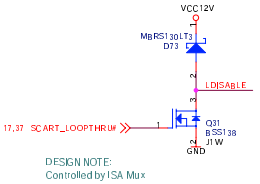
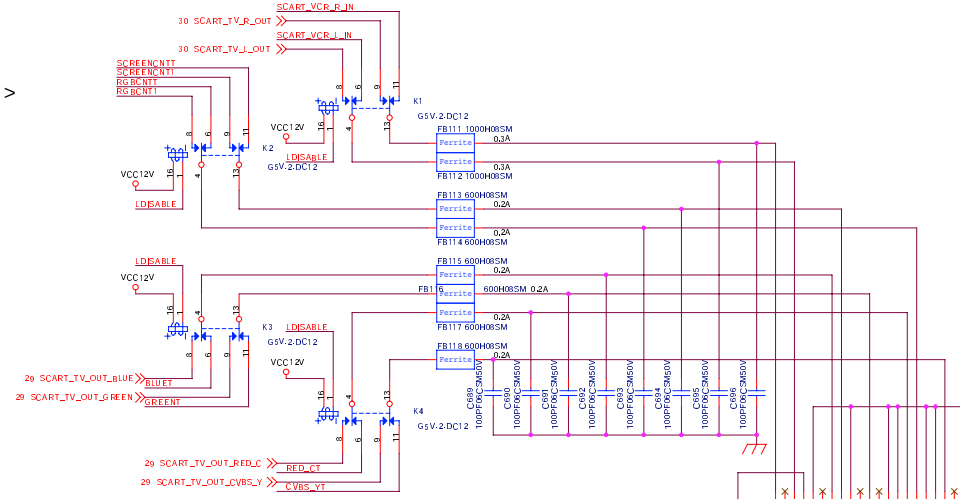


160mA - >

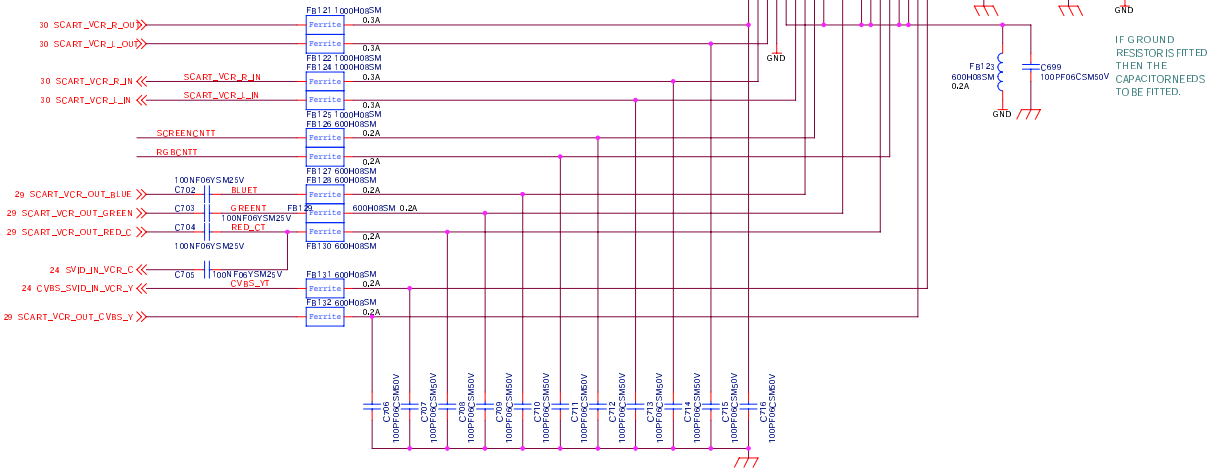


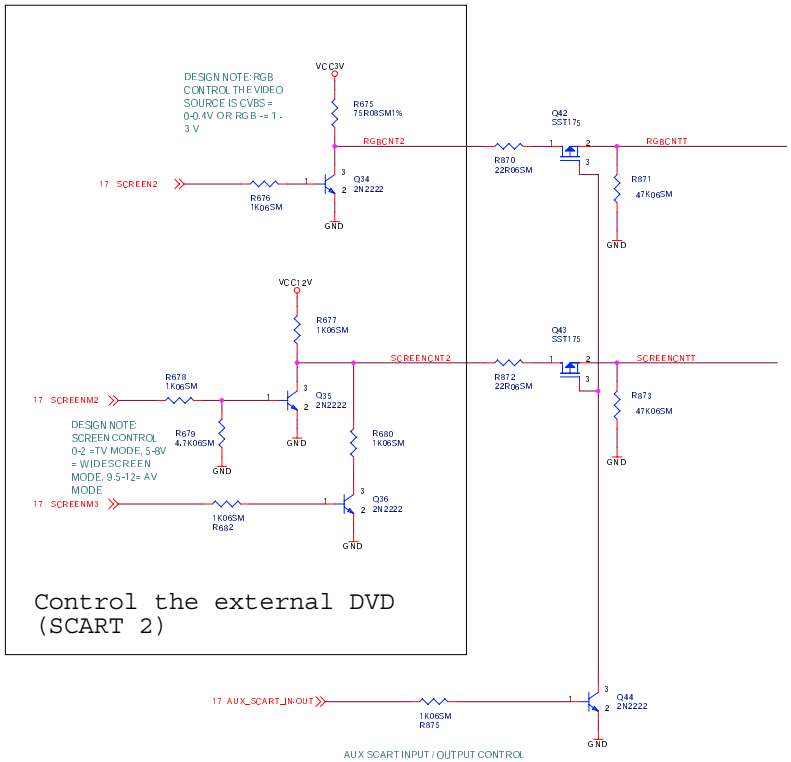


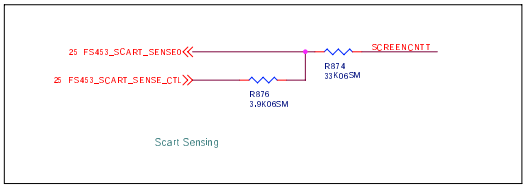
SCART 1 OUT TV (TOP) SK14 22 - 42

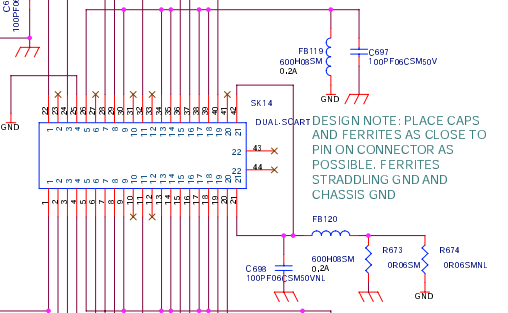
SCART 2 IN/OUT VCR (BOTTOM) SK14 1 -21

BACK PANEL









DUAL SCART

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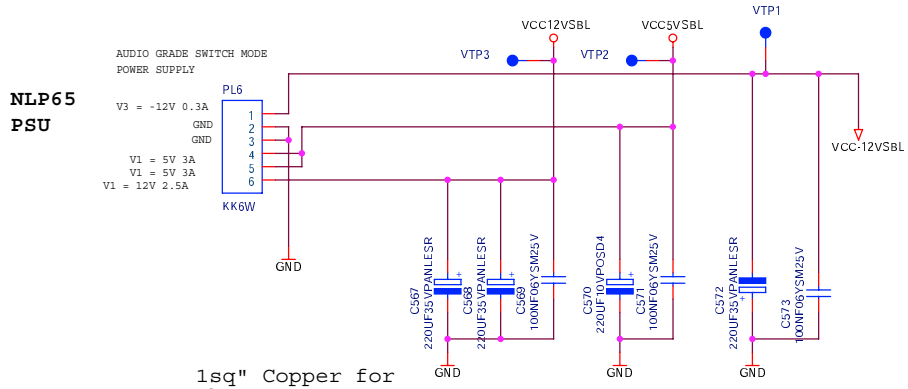
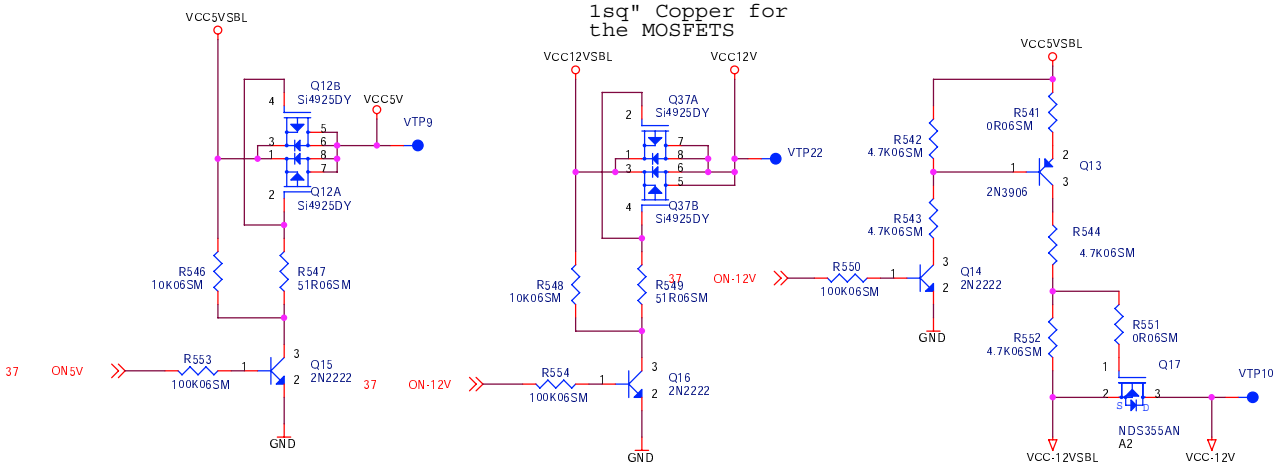
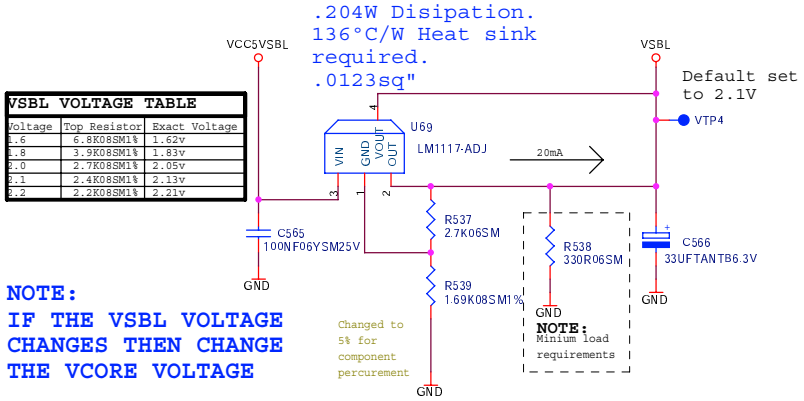
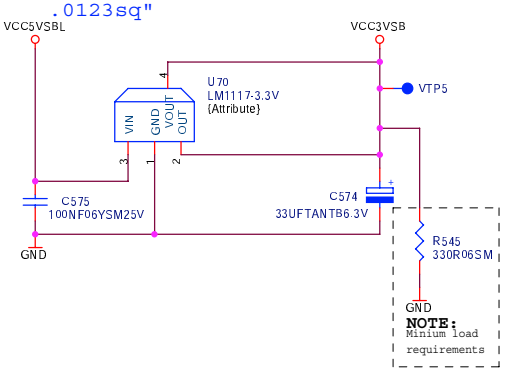
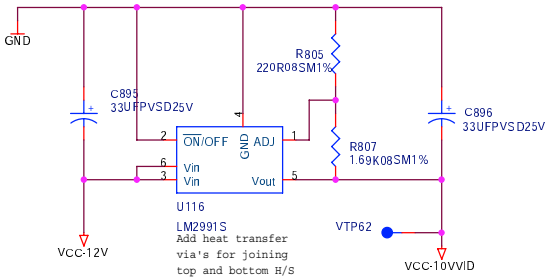
MISCELLANEOUS REGULATORS AND POWER IN

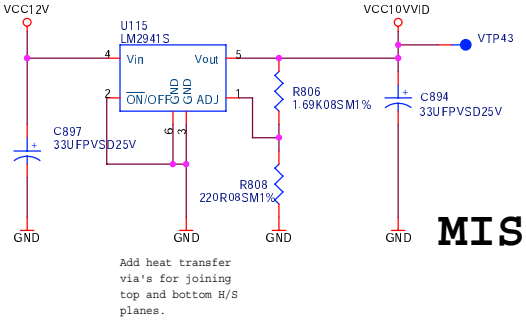


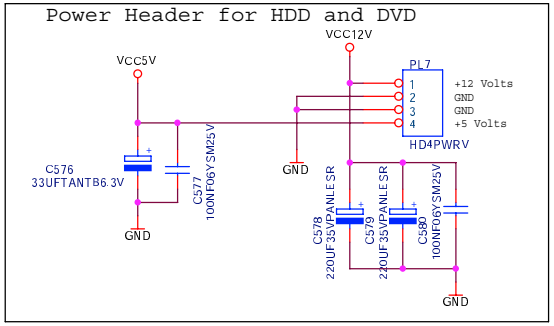












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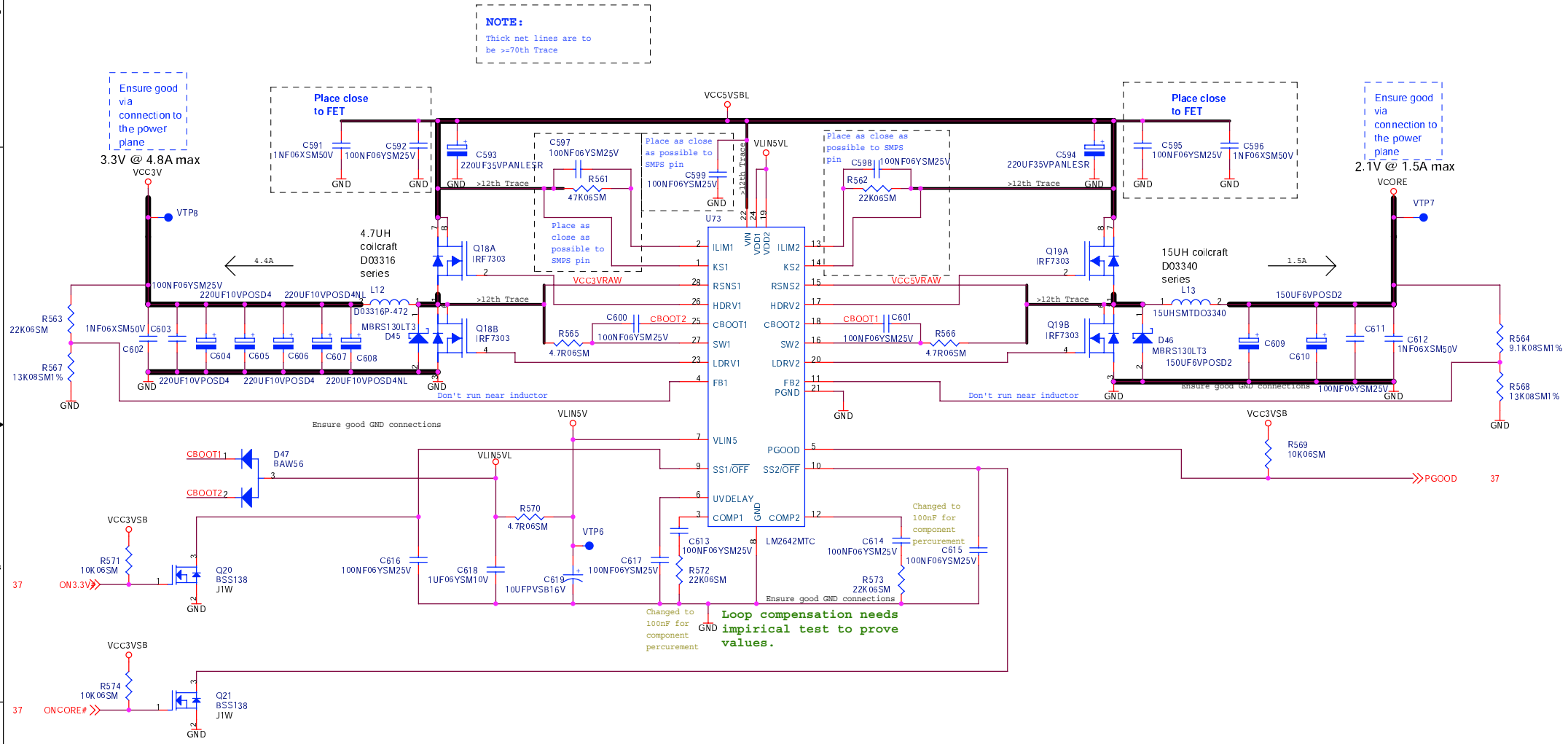

3.3V & VCORE SMPS

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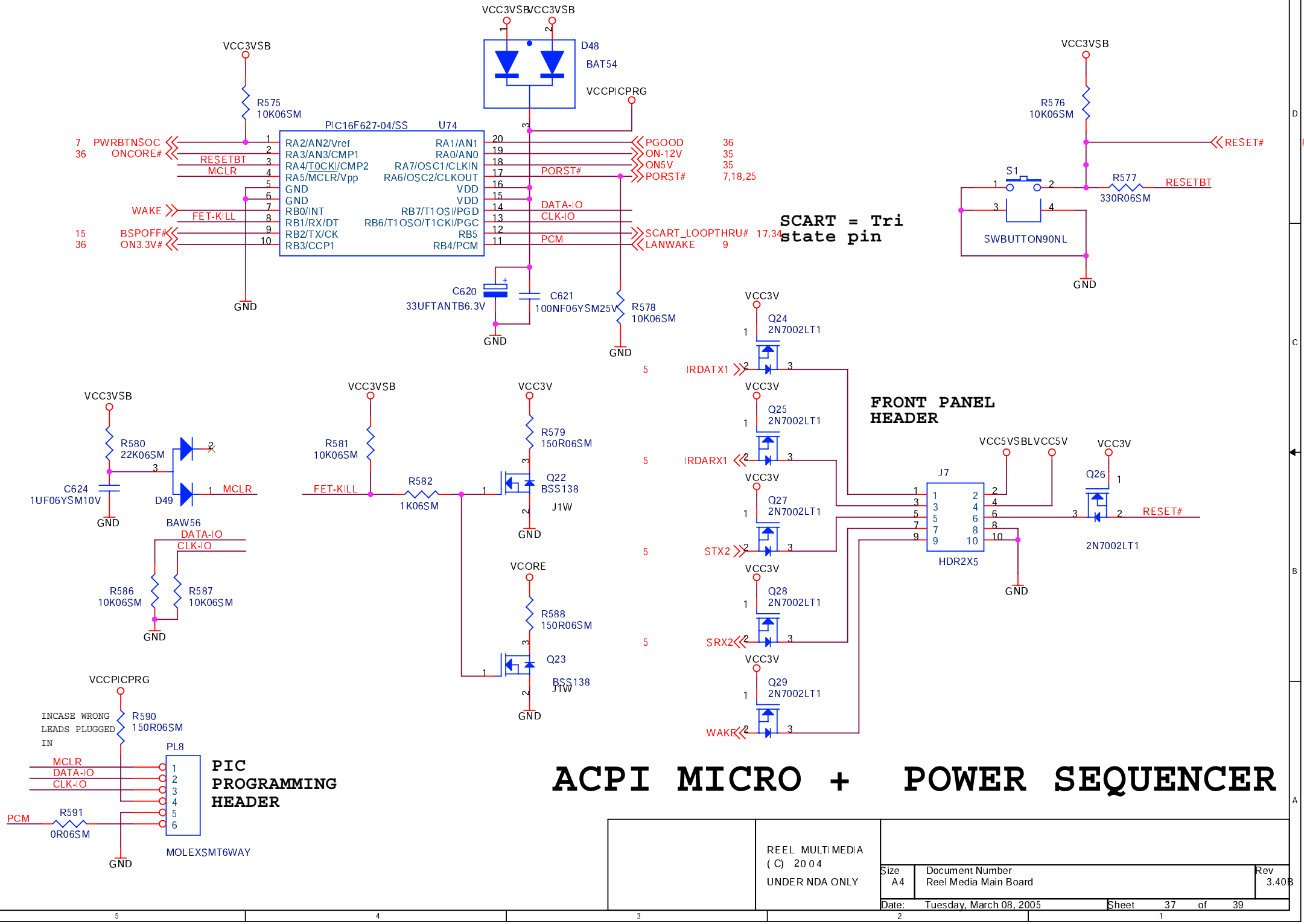
VCC3VSB
D48
BAT54
VCCPICPRG
R575
10K06SM
PIC16F627-04/SS
U74
7 PWRBTNSOC
36 ONCORE#
RESETBT
MCLR
WAKE
FET-KILL
15 BSPOFF#
36 ON3.3V#
RA2/AN2/Vref
RA3/AN3/CMP1
RA4/T0CKI/CMP2
RA5/MCLR/Vpp
GND
GND
RB0/INT
RB1/RX/DT
RB2/TX/CK
RB3/CCP1
RA1/AN1
RA0/AN0
RA7/OSC1/CLKIN
RA6/OSC2/CLKOUT
VDD
VDD
RB7/T1OSI/PGD
RB6/T1OSO/T1CKI/PGC
RB5
RB4/PCM
PGOOD 36
ON-12V 35
ON5V 35
PORST# 7,18,25
PORST#
DATA-IO
CLK-IO
SCART_LOOPTHRU# 17,34
LANWAKE 9
PCM
C620
33UFTANTB6.3V
C621
100NF06YSM25V
R578
10K06SM
GND
VCC3VSB
R576
10K06SM
RESET#
S1
R577
330R06SM
RESETBT
SWBUTTON90NL
GND
SCART = Tri state pin
VCC3V
Q24
2N7002LT1
5 IRDATX1
VCC3V
Q25
2N7002LT1
5 IRDARX1
VCC3V
Q27
2N7002LT1
5 STX2
VCC3V
Q28
2N7002LT1
5 SRX2
VCC3V
Q29
2N7002LT1
WAKE
FRONT PANEL HEADER
J7
HDR2X5
VCC5VSBL
VCC5V
VCC3V
Q26
2N7002LT1
RESET#
GND
VCC3VSB
R580
22K06SM
C624
1UF06YSM10V
D49
MCLR
BAW56
DATA-IO
CLK-IO
R586
10K06SM
R587
10K06SM
GND
VCC3VSB
R581
10K06SM
FET-KILL
R582
1K06SM
VCC3V
R579
150R06SM
Q22
BSS138
J1W
GND
VCORE
R588
150R06SM
Q23
BSS138
J1W
GND
VCCPICPRG
INCASE WRONG LEADS PLUGGED IN
R590
150R06SM
PL8
MCLR
DATA-IO
CLK-IO
PCM
R591
0R06SM
MOLEXSMT6WAY
GND
PIC PROGRAMMING HEADER
ACPI MICRO + POWER SEQUENCER
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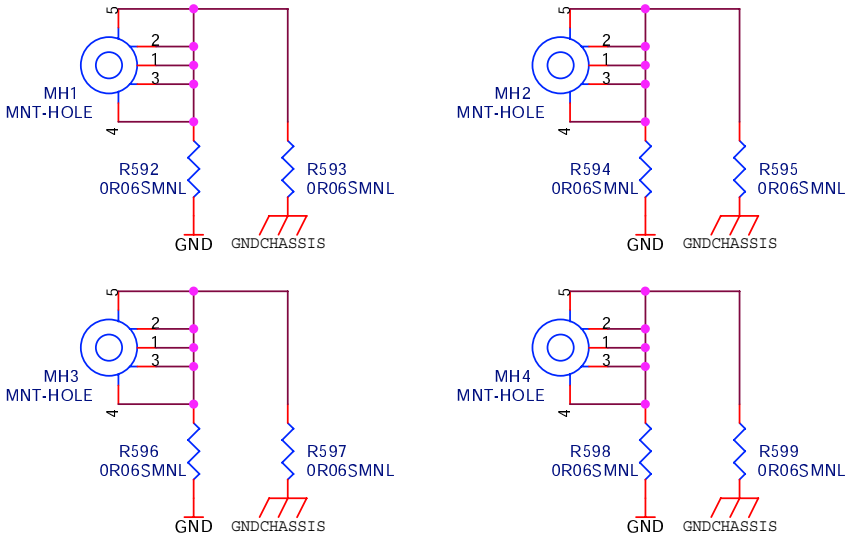

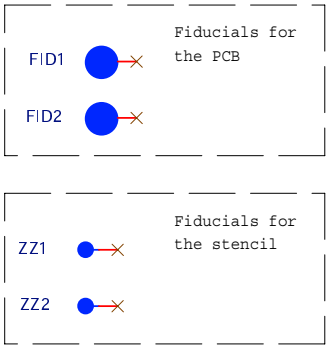

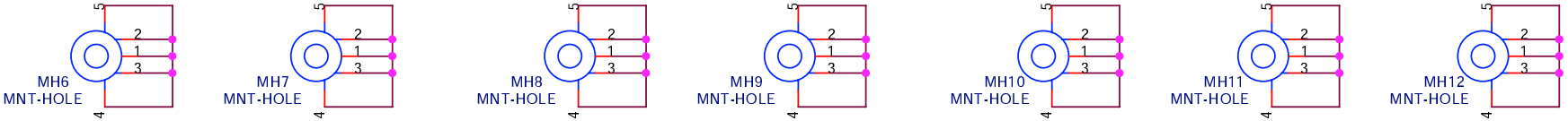

MOUNTING HOLES

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UNDER INVESTIGATION

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